EE 505

Lecture 25

ADC Design

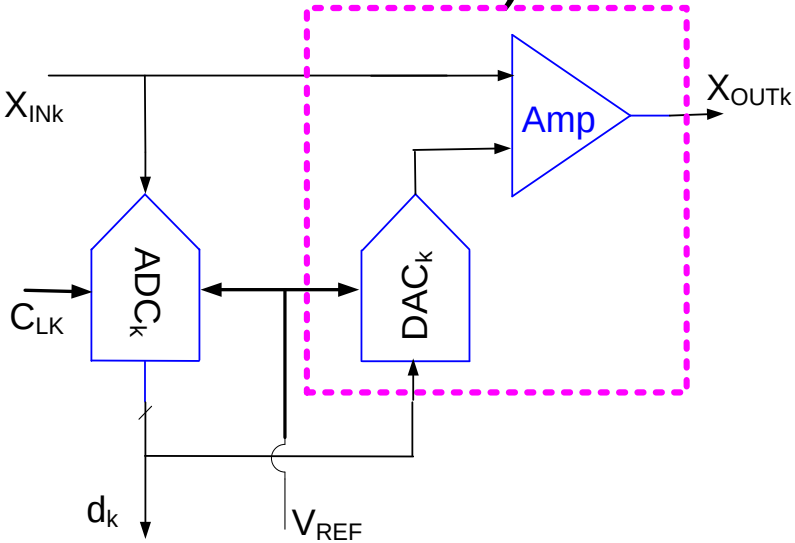
- Pipeline

Review from last lecture

Performance Limitations

(consider amplifier, ADC and DAC issues)

- ADC
  - Break Points (offsets)
- DAC
  - DAC Levels (offsets)
    - Out-range (over or under range)
- Amplifier
  - Offset voltages
  - Settling Time
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Inadequate open loop gain
    - Component mismatch
  - Power Dissipation
  - kT/C switching noise



Review from last lecture

How Much Gain?

Depends upon how much of the overall error budget is allocated to the effect noninfinite gain has on required performance parameters

If require n ENOB, can ½ LSB be allocated to effects of op amp gain error?

e.g. If INL specification of a 12-bit ADC is ½ LSB, can ½ LSB be allocated to the noninfinite gain error?

Sources that may contribute to INL errors in pipelined ADC:

Finite Op Amp Gain
Capacitor Missmatch
Incomplete amplifier settling
Amplifier nonlinearity
Input S/H error
Parasitic capacitance nonlinearity
Offset voltage (in ADC, DAC, summer)
DAC errors
ADC nonlinaritry

Review from last lecture

Error Budgeting

Sources that may contribute to INL errors in pipelined ADC:

Finite Op Amp Gain
Capacitor Missmatch
Incomplete amplifier settling
Amplifier nonlinearity
Input S/H error
Parasitic capacitance nonlinearity
Offset voltage (in ADC, DAC, summer)
DAC errors
ADC nonlinaritry

If entire error budget (e.g. ½ LSB) is allocated to the Finite Op Amp Gain, what error budget must be allocated to all remaining contributors?

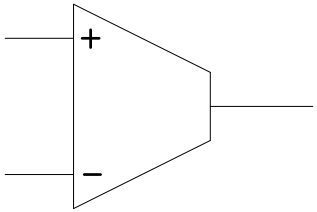
What will happen if each error source is allocated an error budget of (e.g. ½ LSB)?

How should the error sources contribution to overall error budget be allocated?

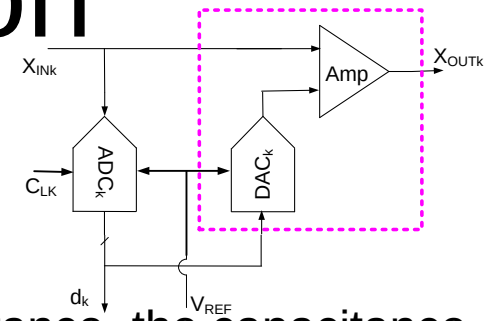
$$\sum_{i=1}^{m} e_i = \frac{1}{2} LSB$$ (maybe a little bit overly conservative)

Review from last lecture

Power Dissipation



$$GB = \frac{g_{mT}}{C_L}$$



C_L is the parallel combination of any interconnect capacitance, the capacitance of the β network and the sampling capacitance of the following stage

For MOS implementation (with ref SE op amp or telescopic cascade op amp)

$$GB = \frac{2I_{DQ}}{V_{EB}C_L} = \left(\frac{1}{(V_{DD}-V_{SS})}\frac{P}{C_L}\right)\frac{1}{V_{EB}}$$

For convenience, define

$$V_{SUP} = V_{DD} - V_{SS}$$

$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$

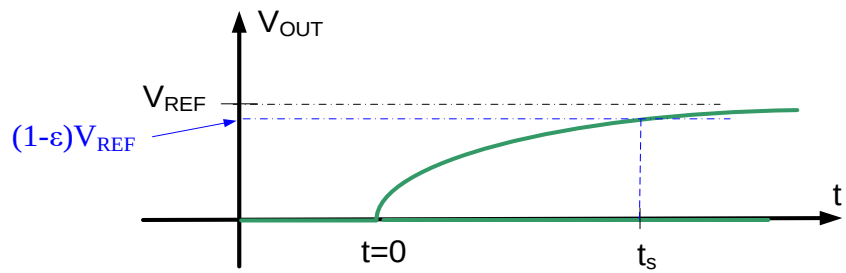
- P increases linearly with GB
- Keep V_{EB} small, C_L as small as possible, GB as small as possible
- At high speeds, diffusion parasitics will cause P to increase more rapidly than GB
- Total amplifier power is sum of power in each stage

Review from last lecture

Settling Time

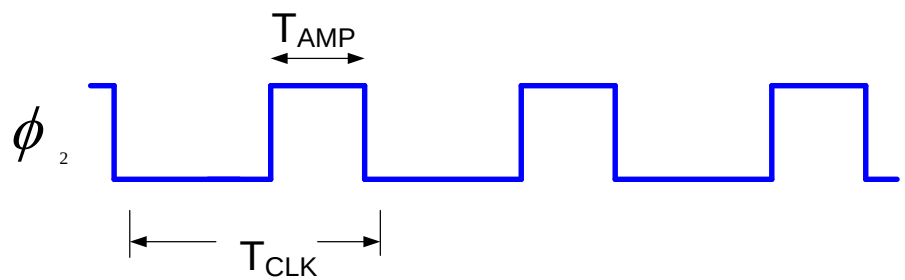
Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step in each stage

Step response (if slewing is neglected)



Design requirements for GB of Op Amp

$$t_s \cong \frac{0.7(n_{ST}+1)}{\beta GB}$$



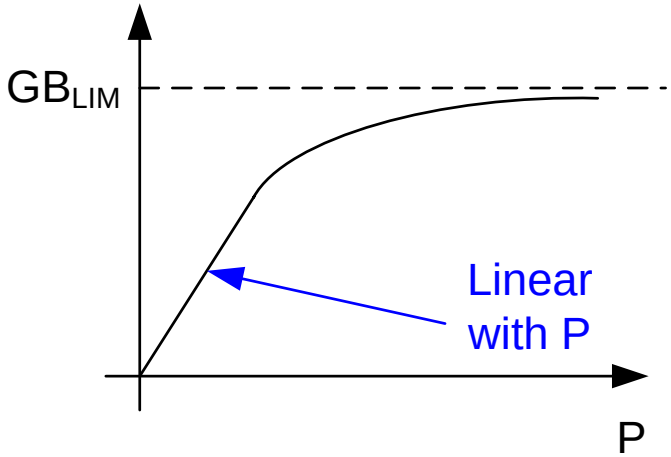
$$t_s = t_{AMP} \cong \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}}$$

$$GB_{RPS} \cong \frac{1.4(n_{ST}+1)}{\beta} f_{CLK} \qquad GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

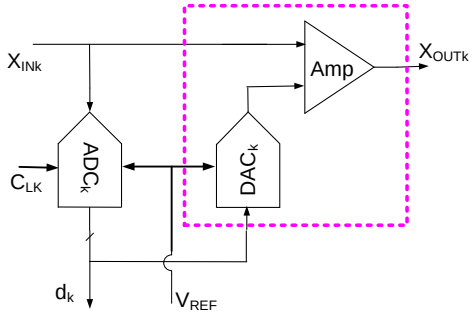
Note: GB requirements drop from stage to stage

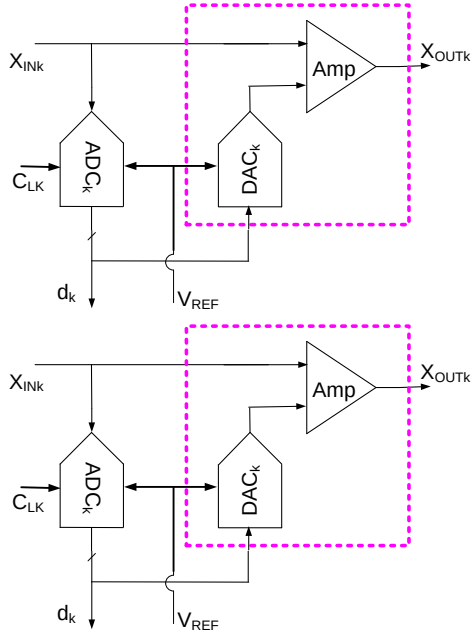
Review from last lecture

Power Dissipation



$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$

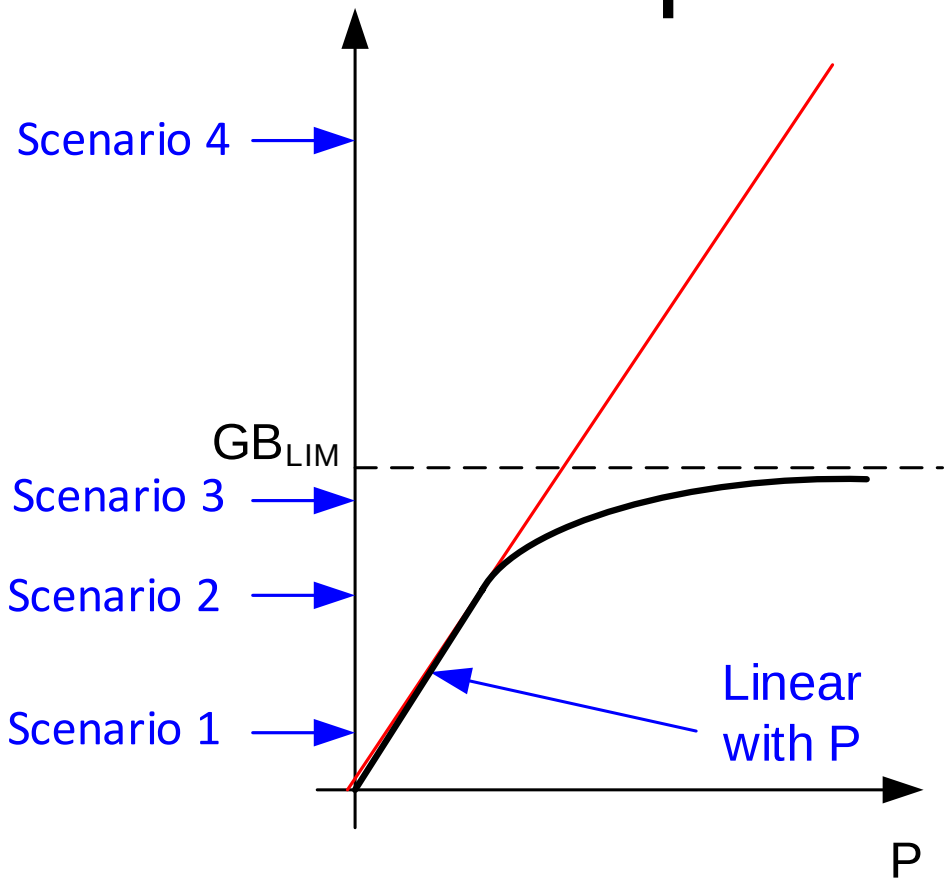




Interleaving can dramatically reduce power requirements (e.g. two interleaved stages reduce GB requirements a factor of 2 on each stage thereby maintaining power requirements on linear slope region) for high speed data converters but introduces some calibration challenge**s**

Review from last lecture

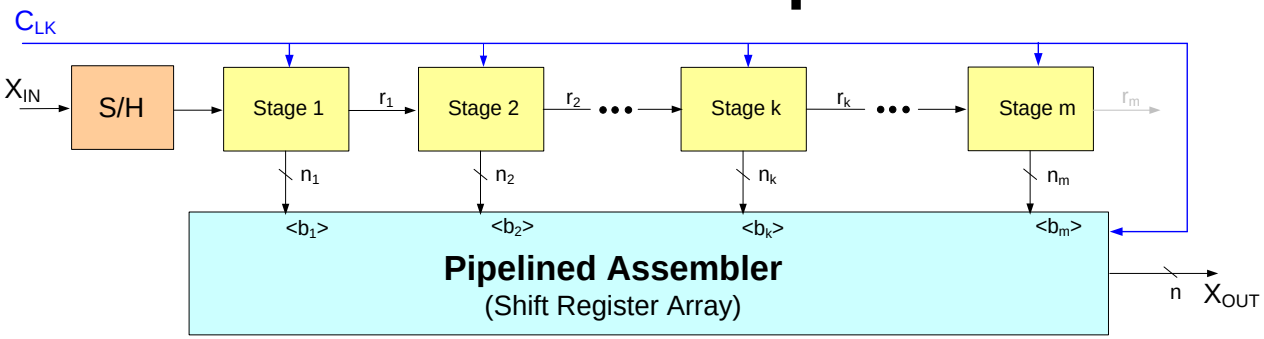
Power Dissipation



GB_{LIM} strongly technology dependent

What do we do if system requirements are in the respective scenarios?

Power Dissipation



Capacitor sizing to meet noise requirements

For each stage: $P=[V_{SUP} \bullet GB \bullet C_L][V_{EB}]$

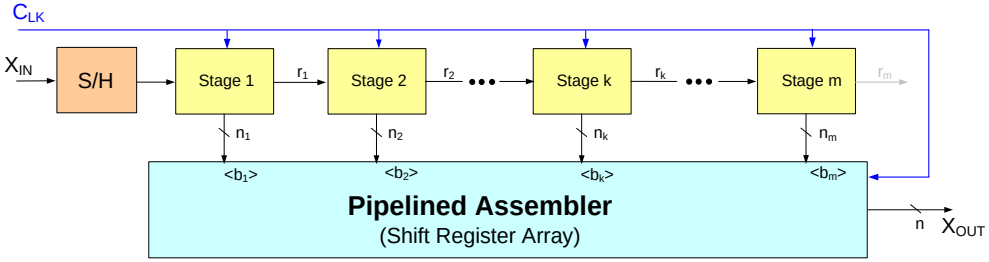
kT/C noise is contributed by each stage

If calibration is used to manage capacitor mismatch, capacitor sizing determined by noise requirements

Should capacitor area be allocated to put dominant noise on input stage or later stages?

If part of the total noise comes from latter stages, size of capacitors on input stage can be reduced

Power Dissipation



$$P=[V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

$$GB_{RPS} \cong \frac{1.4(n_{ST}+1)}{\beta} f_{CLK}$$

$$P=\left[V_{SUP}\frac{1.4}{\beta}f_{CLK}V_{EB}\right]C_L(n_{ST}+1) \Rightarrow P=X_F(n_{ST}+1)C_L$$

Example: How do the op amp power requirements change from one-stage to the next with two bits per stage in a 16-bit pipeline. Assume a charge-redistribution gain stage and the size of the capacitors are scaled to keep the noise contributions the same in each stage. Assume the first stage has a total sampling capacitor of value C_1 and all noise is captured on input samples for each stage

Will keep the dc op amp gain for each stage the same

$$V_{n1} = \sqrt{\frac{kT}{C_1}}$$

$$V_{n2} = \sqrt{\frac{kT}{C_2}}$$

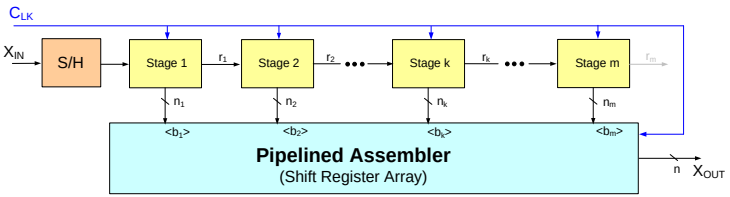
$$V_{n2} = 4V_{n1}$$

$$C_2 = \frac{C_1}{16}$$

$$P_1 = X_F(14+1)C_{L1}$$

$$P_2 = X_F(12+1)\frac{1}{16}C_{L1} \cong 0.05 \bullet P_1$$

Power Dissipation



Example sol continued:

$$P_1 = X_F\,(14+1)\,C_{L1}$$

$$P_2 = X_F\,(12+1)\,\frac{1}{16}\,C_{L1}$$

$$P_3 = X_F\,(10+1)\,\frac{1}{16^2}\,C_{L1}$$

$$P_4 = X_F\,(8+1)\,\frac{1}{16^3}\,C_{L1}$$

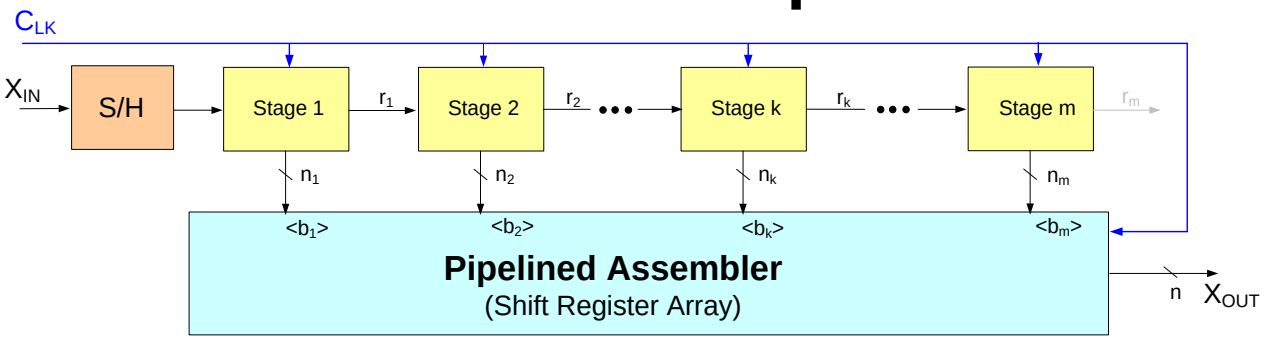
$$P_5 = X_F\,(6+1)\,\frac{1}{16^4}\,C_{L1}$$

$$P_6 = X_F\,(4+1)\,\frac{1}{16^5}\,C_{L1}$$

$$P_7 = X_F\,(2+1)\,\frac{1}{16^6}\,C_{L1}$$

- Power completely dominated by first stage
- Will likely not scale C so much so noise will be dominated by first stage
- No benefit from scaling power in latter stages

Power Dissipation



Capacitor sizing to meet noise requirements

For each stage: $P=[V_{SUP} \bullet GB \bullet C_L][V_{EB}]$

Should capacitor area be allocated to put dominant noise on input stage or later stages?

If part of the total noise comes from latter stages, size of capacitors on input stage can be reduced

An optimal noise distribution strategy should be followed!

Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Op Amp Gain causes finite gain errors and introduces noninearity	2. a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3. Op amp settling must can cause errors	3. Select GB to meet settling requirements (degrade modestly to account for slewing)
4. Power dissipation strongly dependent upon GB of Op Amps	4. Minimize C_L, use energy efficient op amps, share or shut down op amp when not used, scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies. Good (near optimal) noise distribution strategy should be followed.

Power Efficiency and Settling Time Enhancement

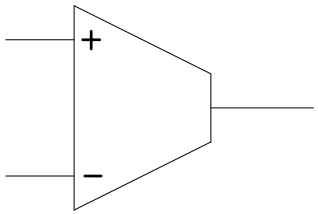
Minimization of Power in Operational Amplifiers

- Reduce Power in Less Significant Stages
- Share Operational Amplifiers Between Stages
- Interleave Amplifiers Between Parallel Paths
- Interleave Pipelined Stages
- Power-Down Operational Amplifiers When Not Used
- Dynamically Bias Operational Amplifiers
- Use Operational Amplifier Architectures that are More Energy Efficient

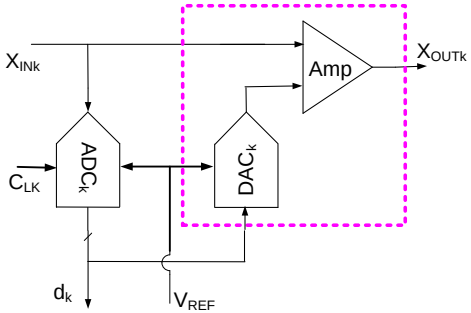
Energy-Efficient Operational Amplifier Architectures?

- Settling Time Inversely Proportional to GB of an OP AMP (during linear settling)
- How does the energy efficiency of GB for various op amps compare?

Power Dissipation



$$GB = \frac{g_m}{C_L}$$

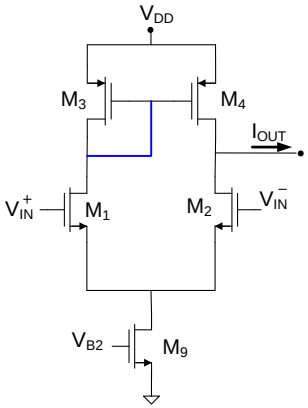


For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

$$P = [V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

Fixed by ADC requirements

Ref SE Op Amp

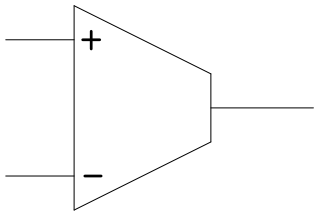


Select architectures that minimize architecture-dependent term

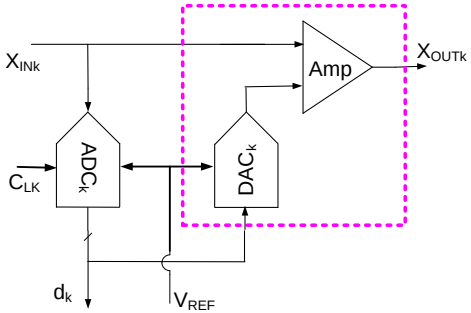
Architecture Dependent

$$GB = \left[\frac{P}{V_{SUP} C_L}\right]\left[\frac{1}{V_{EB}}\right]$$

Power Dissipation



$$GB = \frac{g_m}{C_L}$$

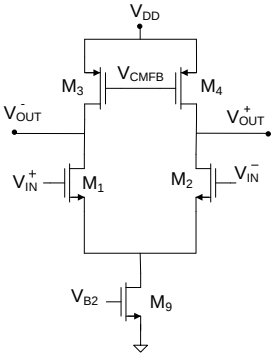


For Single-stage MOS implementation (with ref FD op amp or telescopic cascade op amp)

$$P = \left[V_{SUP} \bullet \frac{GB}{2} \bullet C_L \right] \left[V_{EB} \right]$$

Fixed by ADC requirements

Ref FD Op Amp



Select architectures that minimize architecture-dependent term

Architecture Dependent

$$GB = \left[\frac{2P}{V_{SUP} C_{L\,L}} \right] \left[\frac{1}{V_{EB}} \right]$$

Figure of Merit for Comparing Energy Efficiency of Op Amps

For Single-stage MOS implementation (with ref FD op amp or telescopic cascade op amp)

$$GB = \left[\frac{2 \bullet P}{V_{DD} C_L}\right] \left[\frac{1}{V_{EB}}\right]$$

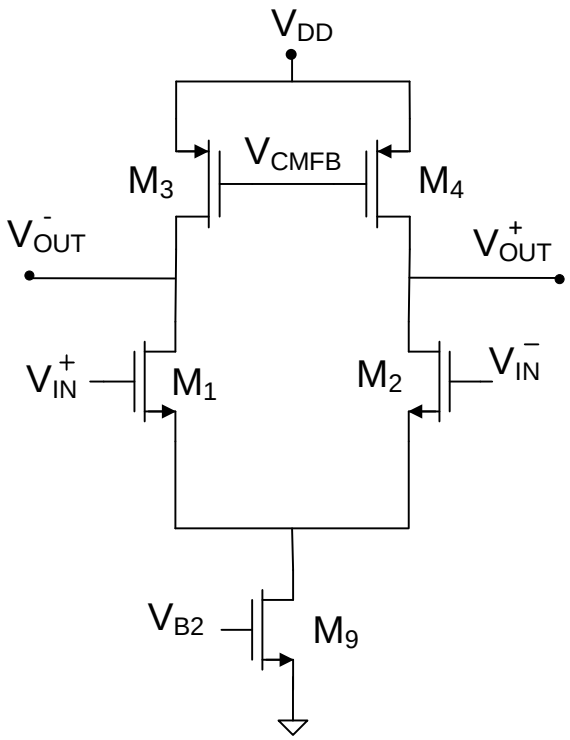
Architecture Independent

Architecture Dependent

$$FOM = \boxed{\frac{GB \bullet V_{SUP} C_L}{2P}}$$

$$FOM_{\text{"Generic MOS Cascode-Type OpAmp"}} = \left[\frac{1}{V_{EB1}}\right]$$

Consider the Basic Single-State FD Op Amp

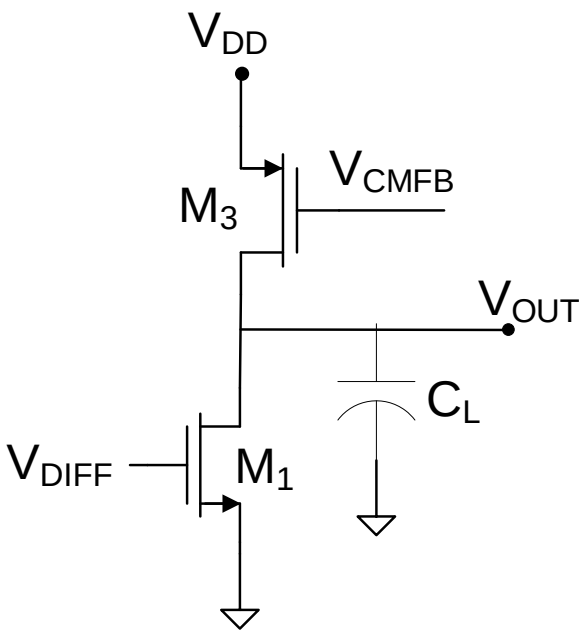


C_L on Differential Outputs Not Shown

CMFB Not Shown

Consider the Basic Single-State FD Op Amp

Differential Half-Circuit



$$A(s) = \frac{-g_{m1}/2}{sC_L + [g_{o3} + g_{o1}]}$$

$$A_O = \frac{g_{m1}/2}{g_{o1} + g_{o3}}$$

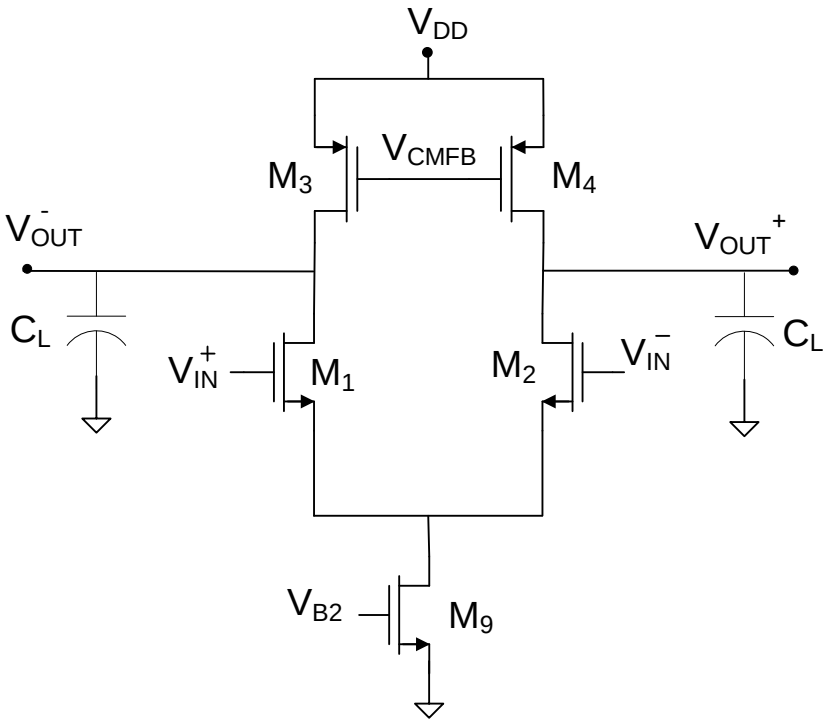
$$BW = \frac{g_{o1} + g_{o3}}{C_L}$$

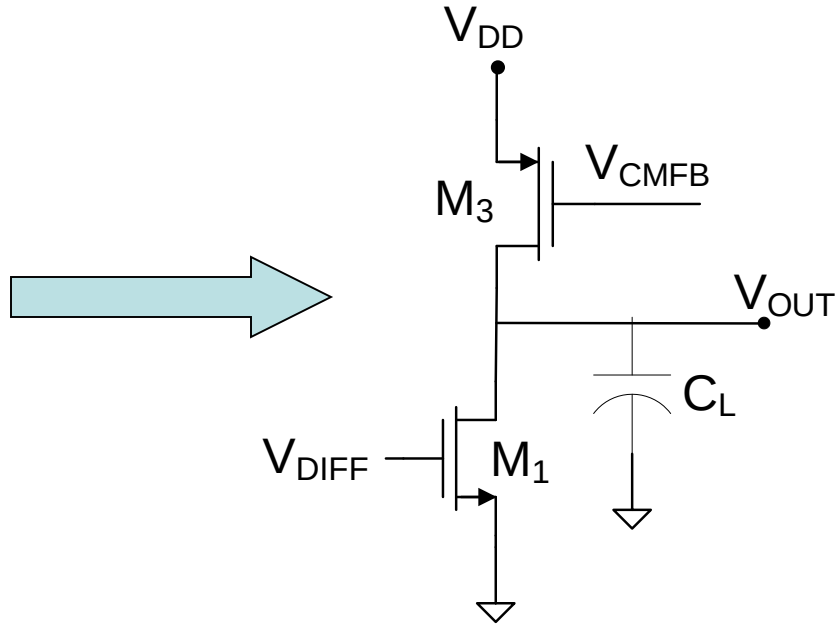
$$GB = \frac{g_{m1}}{2C_L} = \frac{2I_{Q1}}{2V_{EB1}C_L} = \left[\frac{P}{2V_{DD}C_L}\right]\left[\frac{1}{V_{EB1}}\right]$$

$$V_{IN} = \frac{V_{IN}^{+} - V_{IN}^{-}}{2} = \frac{V_{DIFF}}{2}$$

$$\boxed{GB = \left[\frac{P}{2V_{DD}C_L}\right]\left[\frac{1}{V_{EB1}}\right]}$$

Basic Single-Stage FD Op Amp





$$\text{FOM} = \left[\frac{1}{V_{EB1}}\right]$$

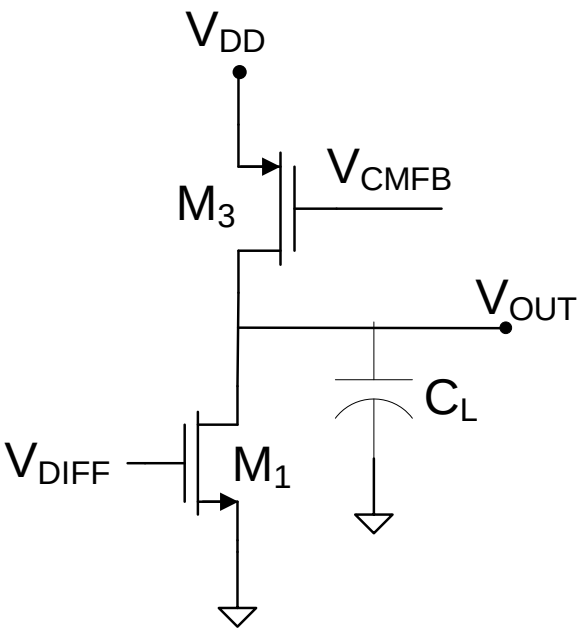
C_L on other output Not Shown

CMFB Not Shown

Consider the Basic Single-Stage FD Op Amp

Differential Half-Circuit

$$GB = \left[\frac{P}{2V_{DD}C_L}\right]\left[\frac{1}{V_{EB}}\right]$$



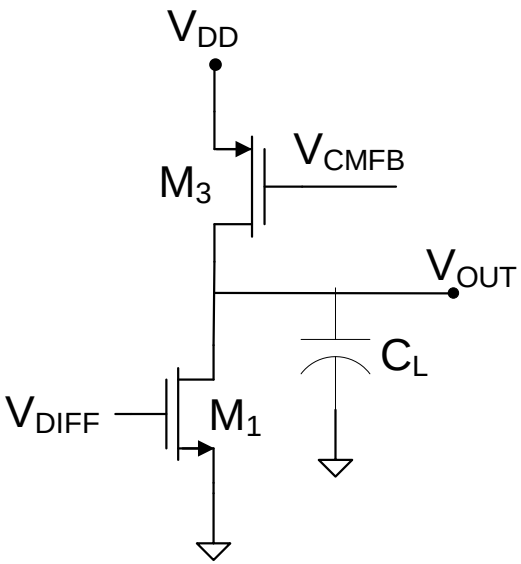
Observations

- GB (settling time) improves linearly with P
- GB (settling time) improves with decreasing V_{EB}

Consider the Basic Single-State Op Amp

Differential Half-Circuit

$$GB = \left[\frac{P}{2V_{DD}C_L}\right]\left[\frac{1}{V_{EB}}\right]$$



Observations

- GB (settling time) improves linearly with P
  Is there any fundamental limit?
- GB (settling time) improves with decreasing V_{EB}
  Conflict with conventional wisdom that speed (f_T) increases with V_{EB}?
- What assumptions implicit to draw these conclusions?
  C_L dominates parasitic capacitances

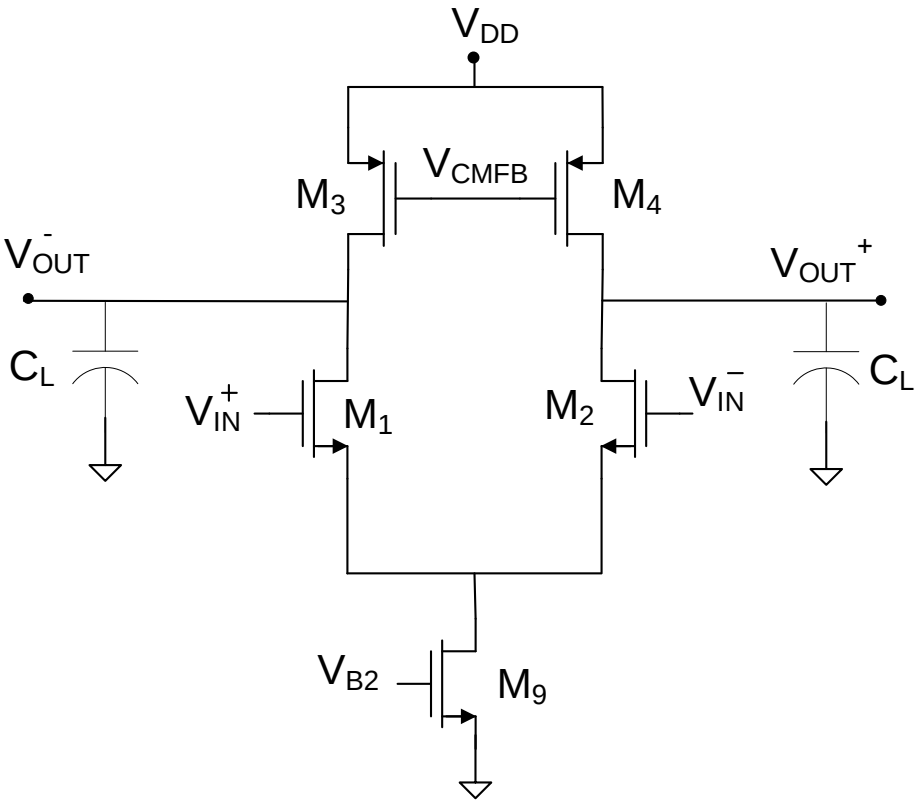
Energy Efficiency of Popular Op Amps

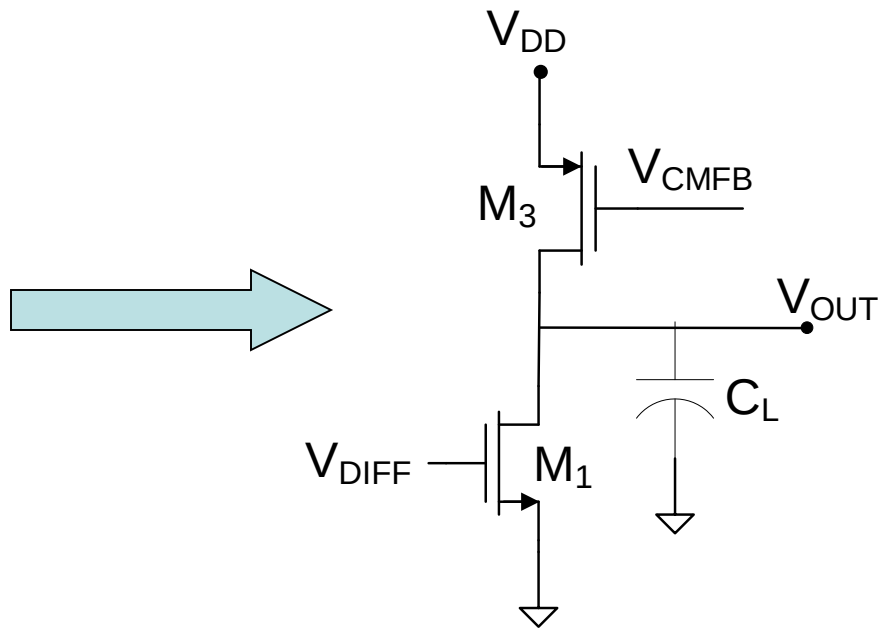
Assume parasitic capacitances on output negligible compared to external load capacitance

Energy Efficiency of Popular Single-Stage Op Amps

- Basic Single-Stage Diff Amp
- Current Mirror Op Amp
- Telescopic Cascode
- Folded Cascode
- Gain-Boosted Telescopic Cascode
- Gain-Boosted Folded Cascode
- -gm Compensated Single-Stage
- Telescopic Cascode Positive Feedback

Basic Single-Stage FD Op Amp



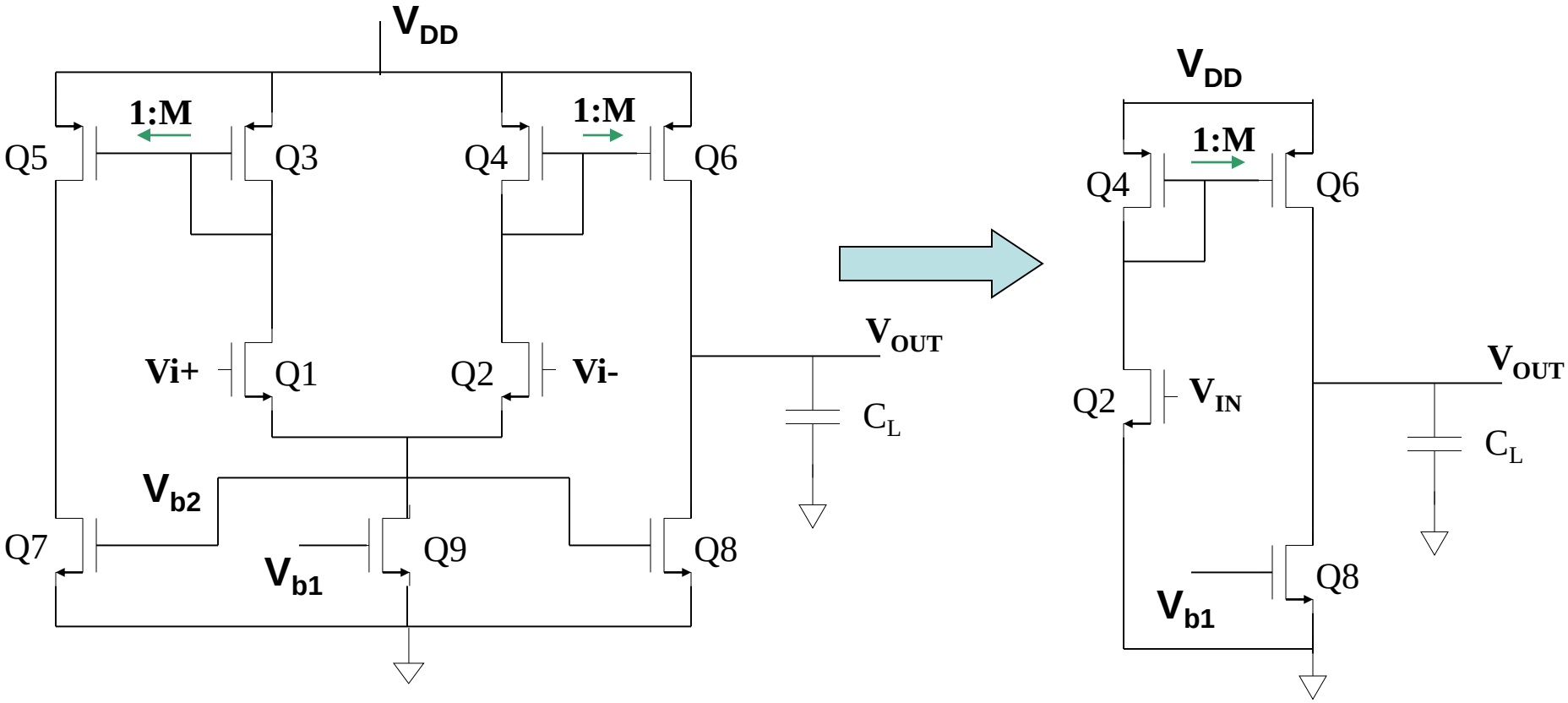


$$\text{FOM} = \left[\frac{1}{V_{EB1}}\right]$$

C_L on other output Not Shown

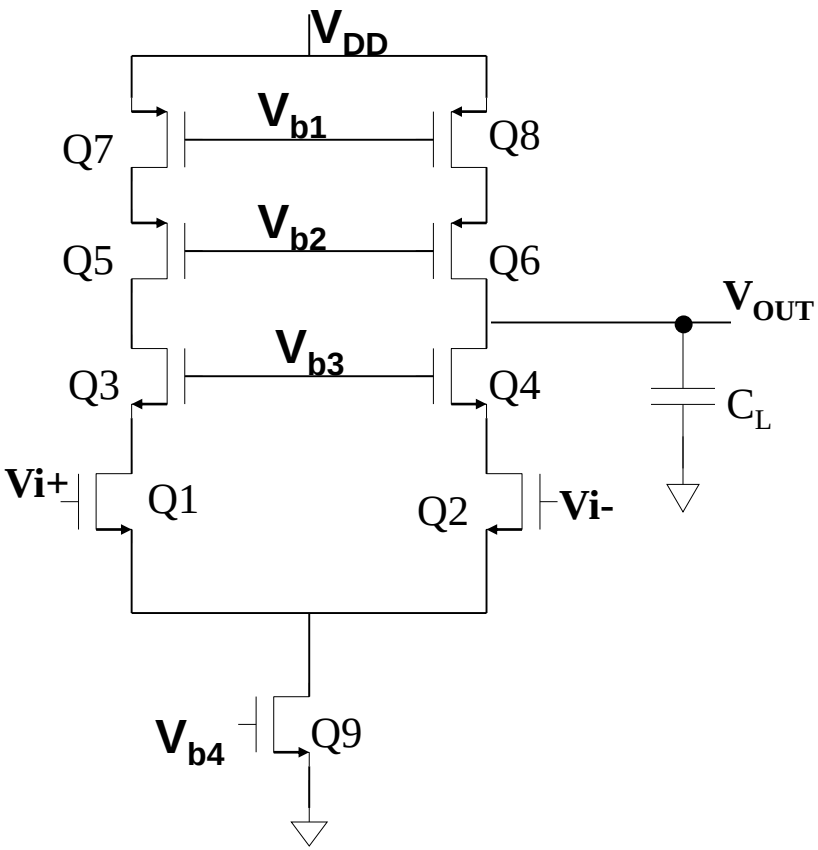
CMFB Not Shown

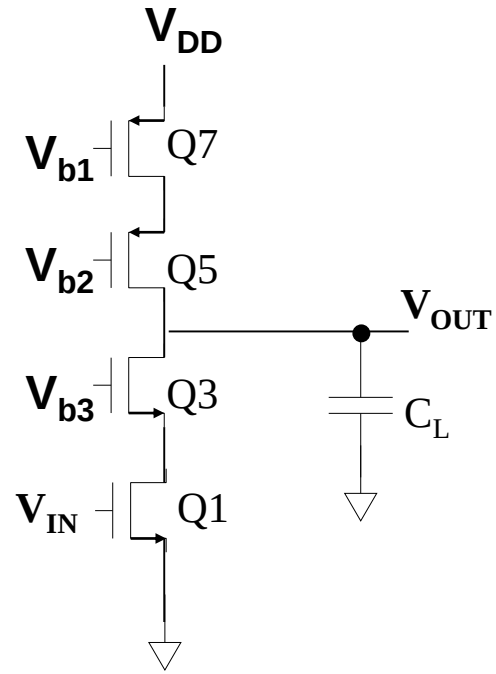
Current Mirror Op Amp



$$\text{FOM} = \left[\frac{M}{M+1}\right]\left[\frac{1}{V_{EB1}}\right]$$

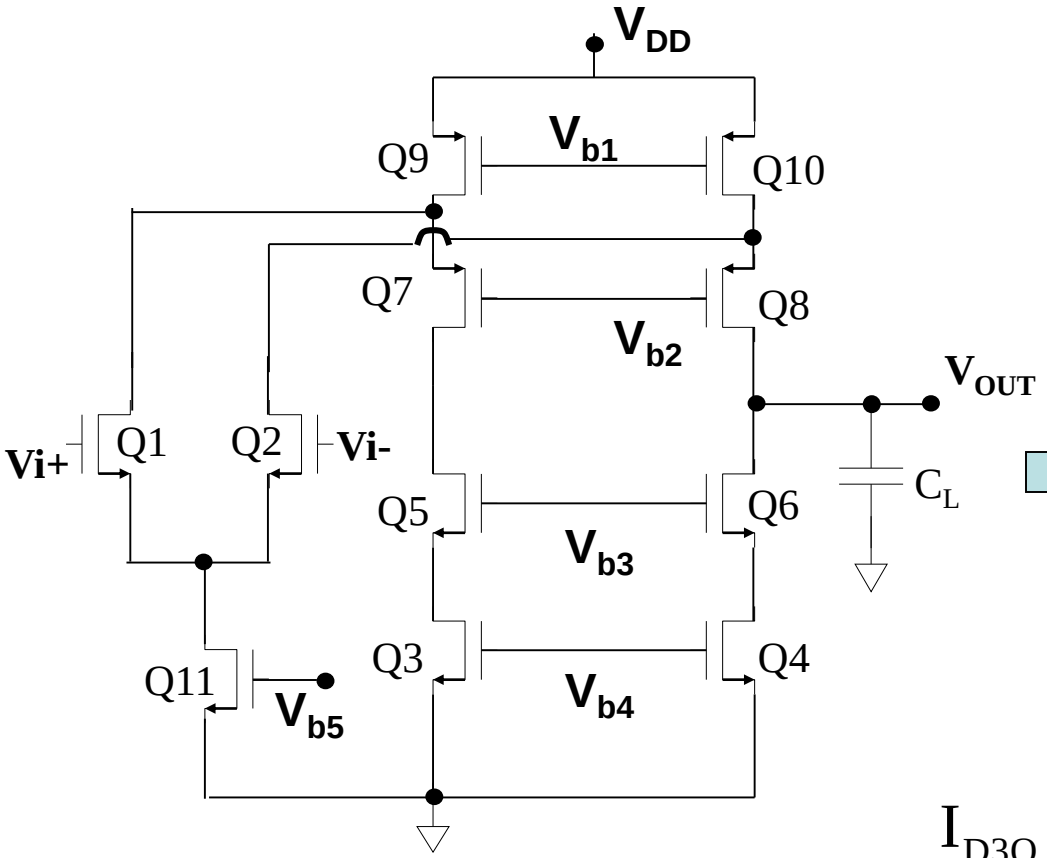
Telescopic Cascode

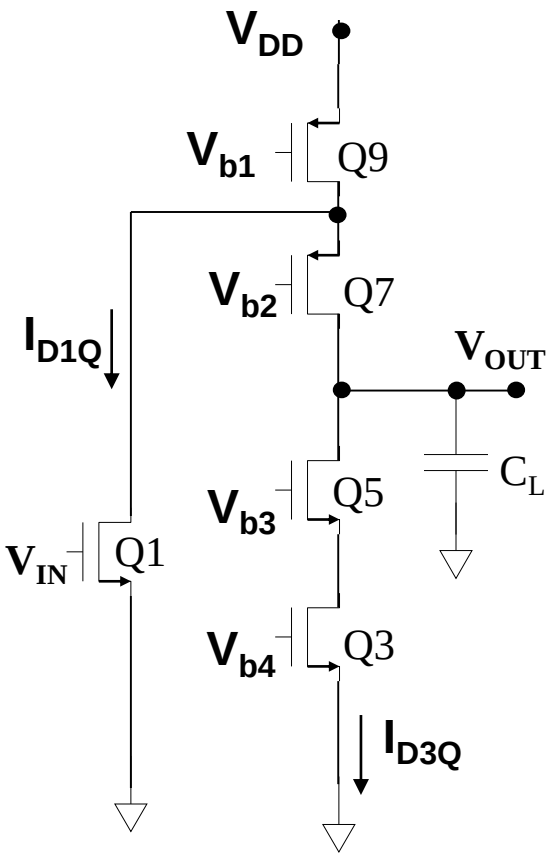




$$\boxed{\mathrm{FOM} = \left[\frac{1}{V_{EB1}}\right]}$$

Folded Cascode

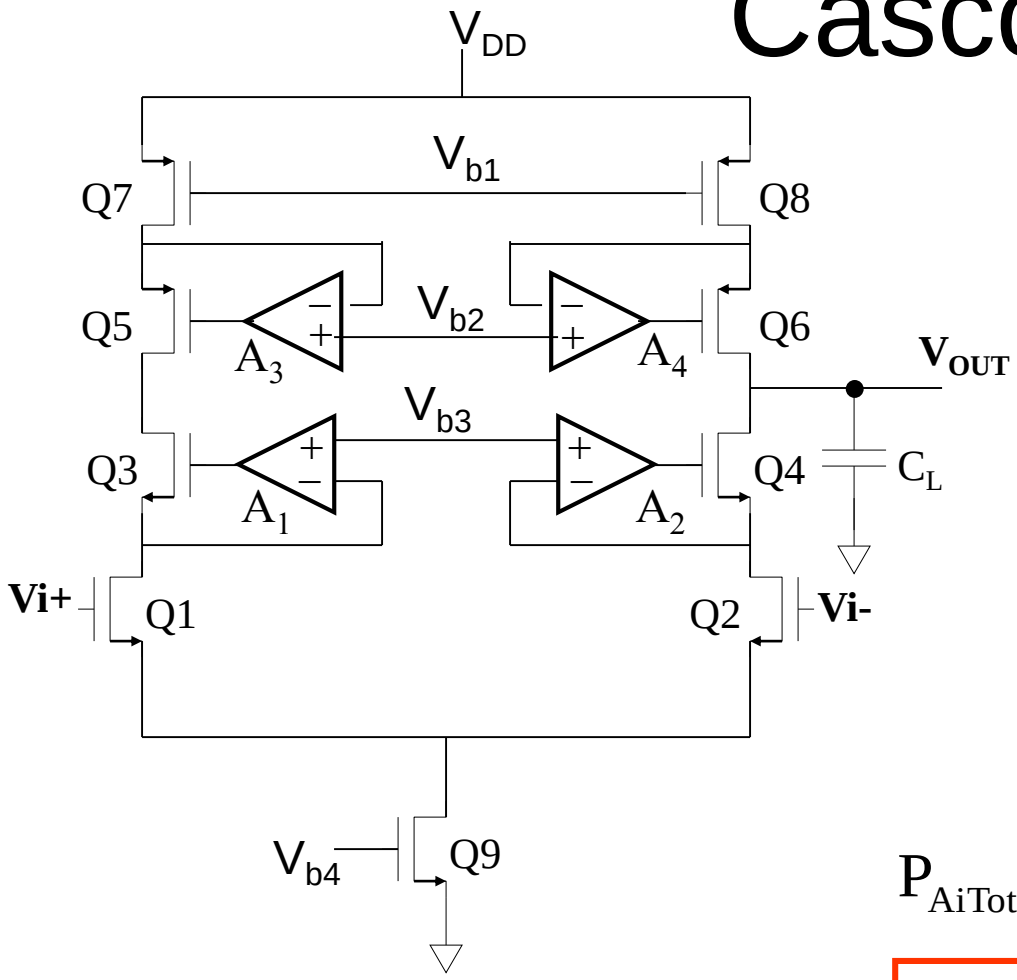


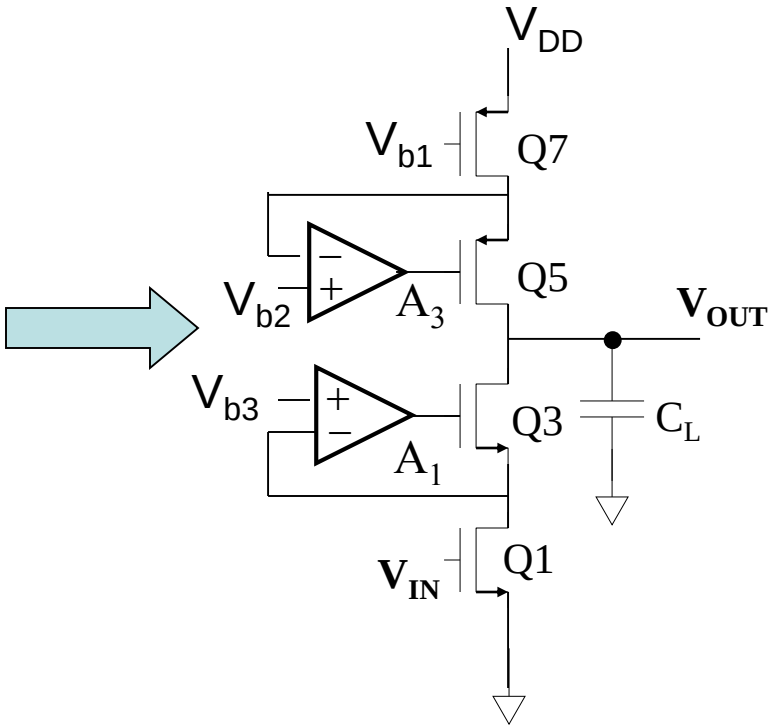


$$I_{D3Q} = \theta I_{D1Q}$$

$$\boxed{\text{FOM} = \left[\frac{1}{1+\theta}\right]\left[\frac{1}{V_{EB1}}\right]}$$

Gain-Boosted Telescopic Cascode

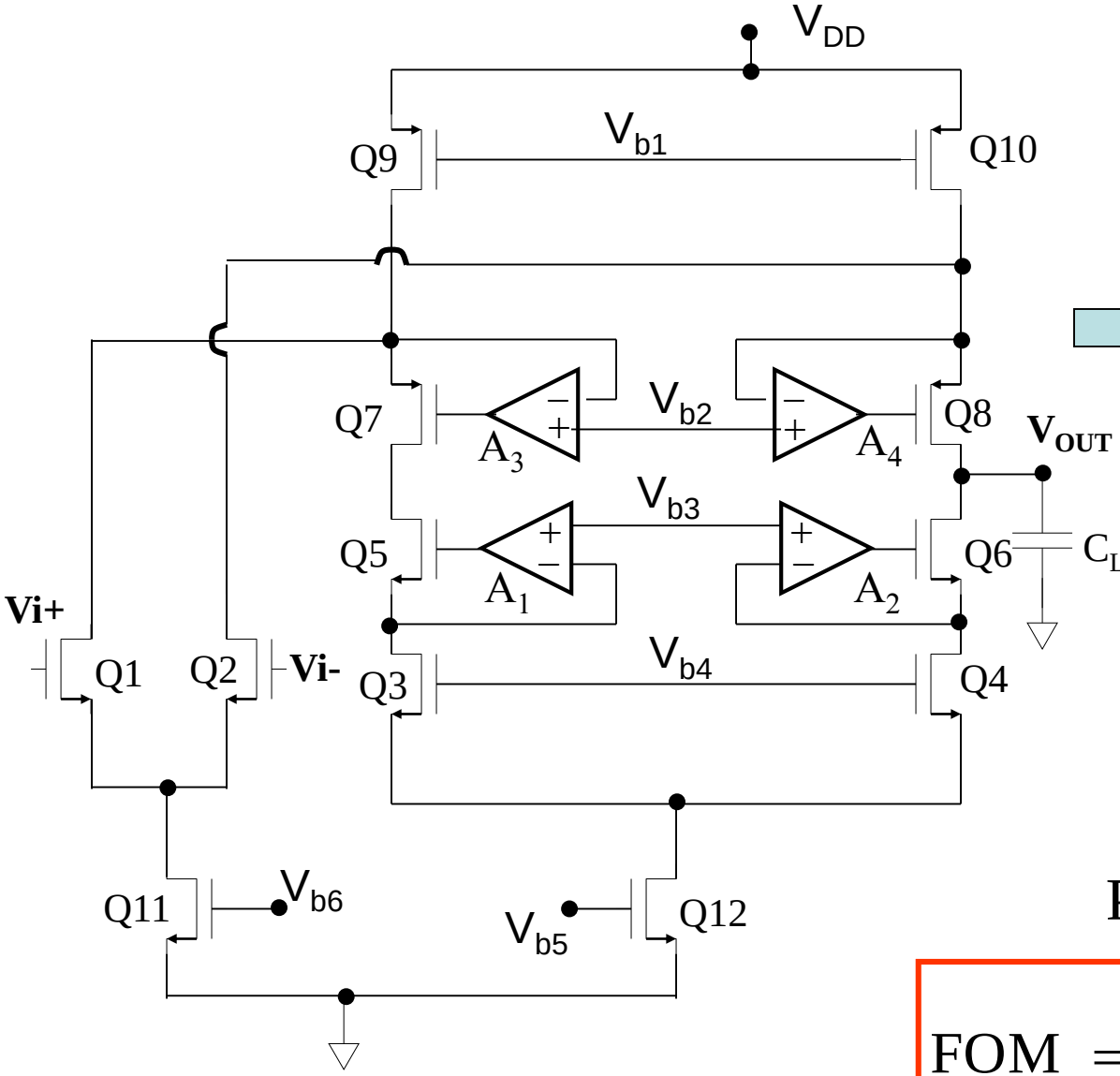


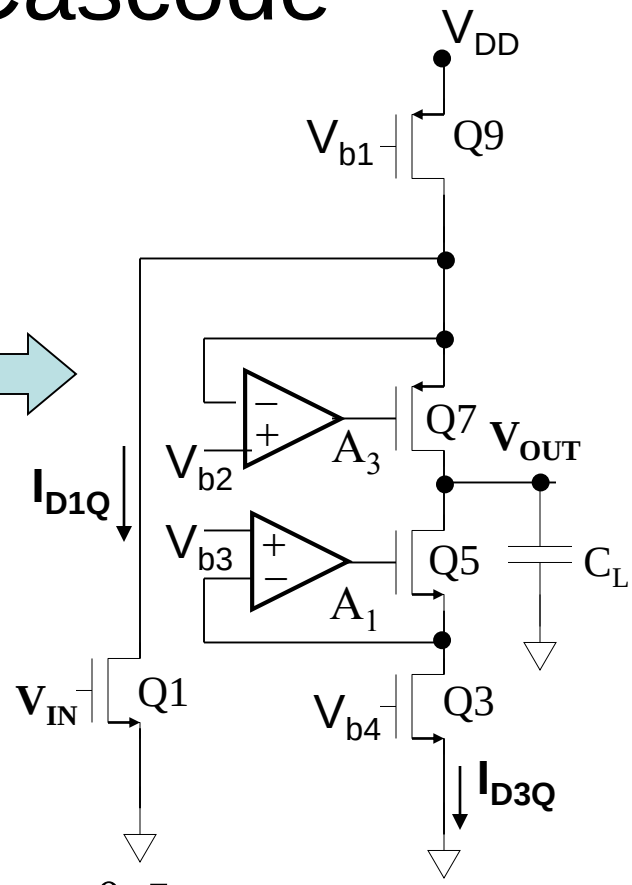


$$P_{AiTotal} = \theta P_{TelescopicCascode}$$

$$\boxed{FOM = \left[\frac{1}{1+\theta}\right]\left[\frac{1}{V_{EB1}}\right]}$$

Gain-Boosted Folded Cascode



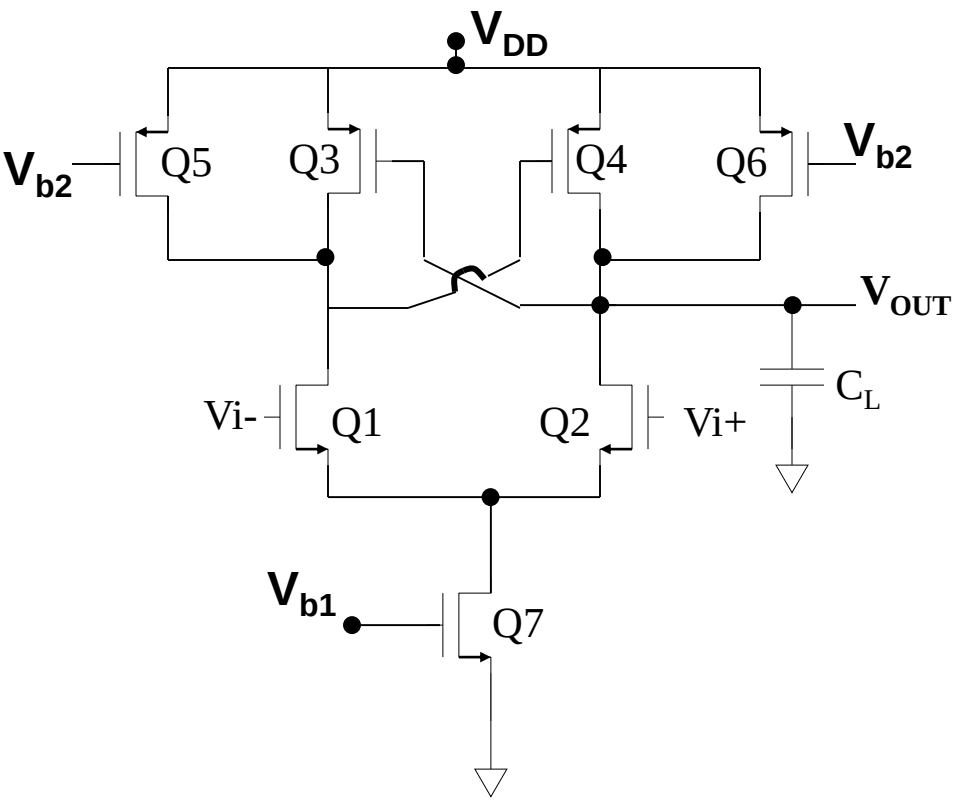


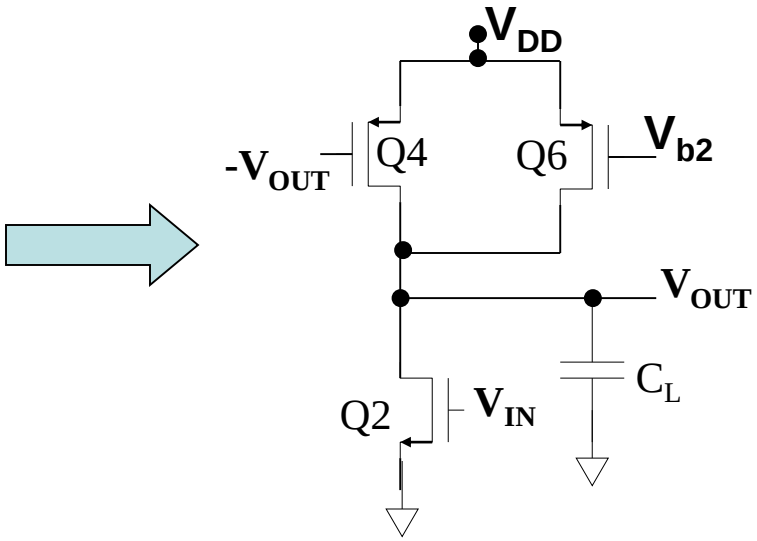
$$I_{D3Q} = \theta_2 I_{D1Q}$$

$$P_{AiTotal} = \theta_1 P_{FoldedCascode}$$

$$\boxed{FOM = \left[\frac{1}{1+\theta_1}\right]\left[\frac{1}{1+\theta_2}\right]\left[\frac{1}{V_{EB1}}\right]}$$

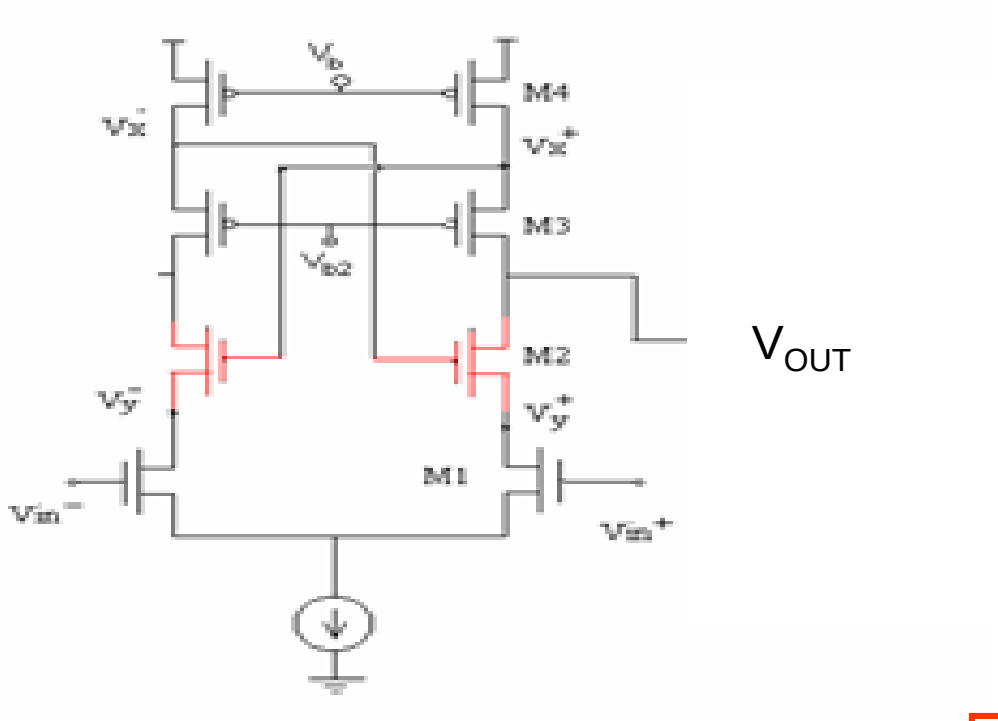
-gm Compensated Single-Stage





$$\text{FOM} = \left[\frac{1}{V_{EB1}}\right]$$

Telescopic Cascode Positive Feedback Op Amp



$$A_v \approx \frac{-g_{m1} \cdot g_{m2} \cdot g_{m3}}{g_{o1}\left(g_{o2} \cdot g_{m3} - g_{o3} \cdot g_{m2}\right)}$$

$$\boxed{\text{FOM} = \left[\frac{1}{V_{EB1}}\right]}$$

Energy Efficiency of Popular Op Amps

- All of the Op Amps in the comparison have an energy efficiency for a given settling requirement that is, at best, as good as that of the basic simple structure if the parasitics are small compared to C_L
- The settling time of most of the amplifiers decreases linearly with P (i.e. improves linearly with P)
- The linear settling time is minimized if V_{EB1} is minimized!

Settling Energy Efficiency of Popular Op Amps

Questions:

- Are there any structures that are more settling energy efficient than the basic amplifier?
- Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?
- Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

Settling Energy Efficiency of Popular Op Amps

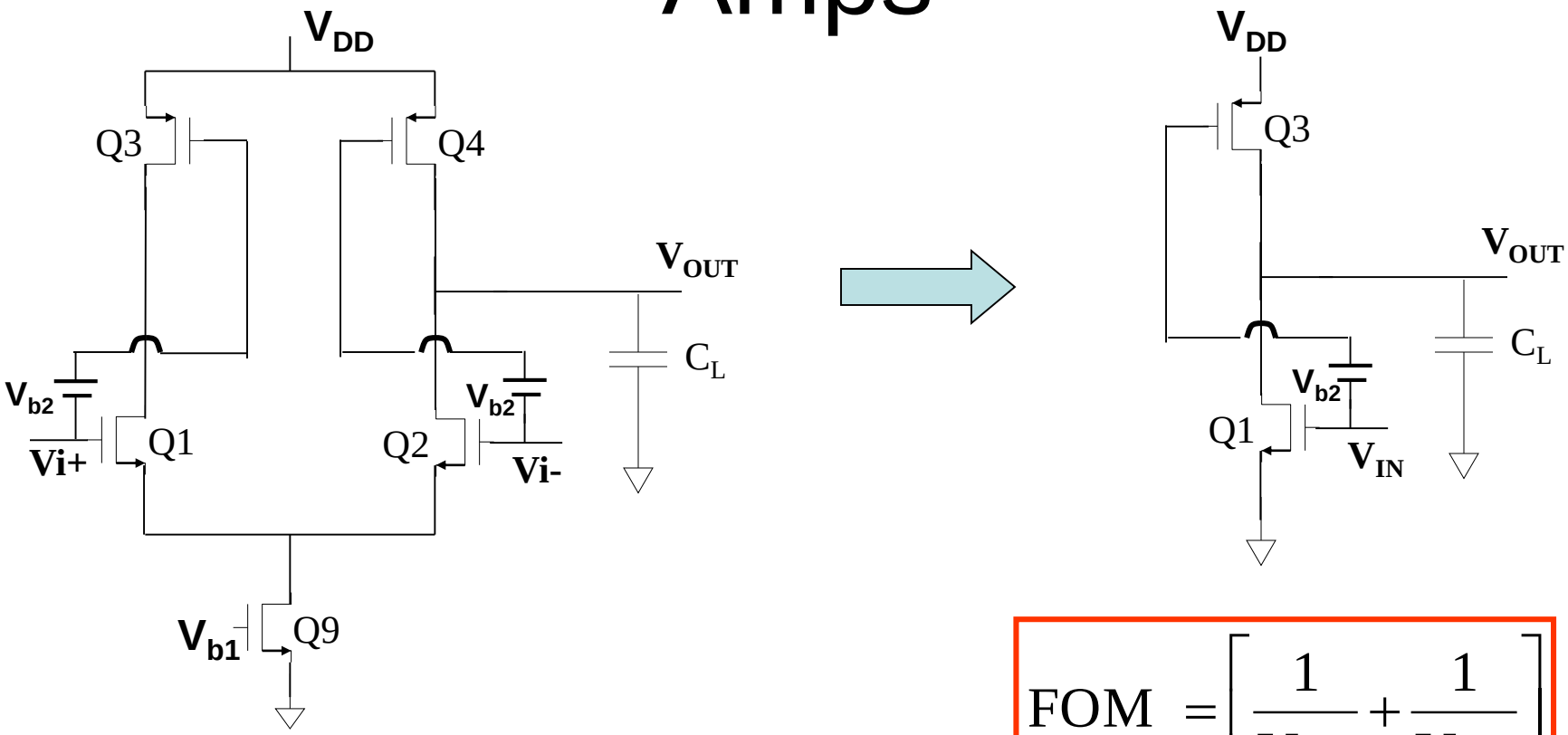
Questions:

- Are there any structures that are more settling energy efficient than the basic amplifier?

- Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

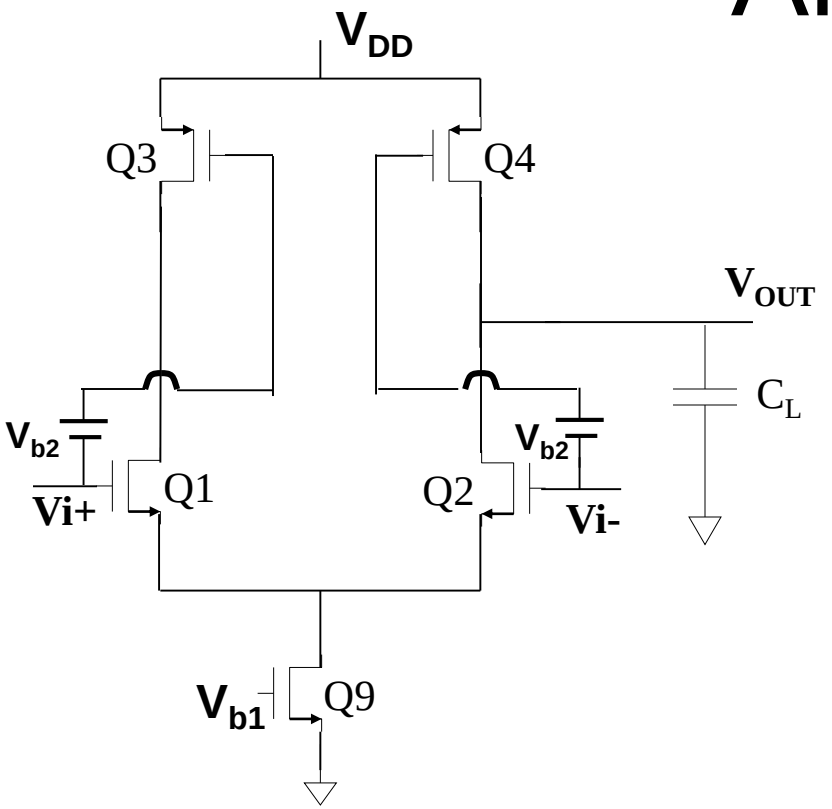
- Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

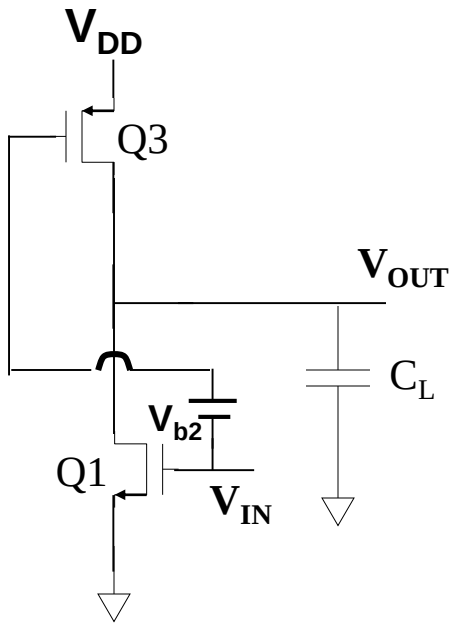
Improved Energy Efficiency Op Amps



$$\text{FOM} = \left[\frac{1}{V_{EB1}} + \frac{1}{V_{EB3}} \right]$$

Improved Energy Efficiency Op Amps





$$\text{FOM} = \left[\frac{1}{V_{EB1}} + \frac{1}{V_{EB3}} \right]$$

Another was presented at ISCAS 2001 - Amourah

There may be more (will consider two-stage structures in a bit)

Settling Energy Efficiency of Popular Op Amps

Questions:

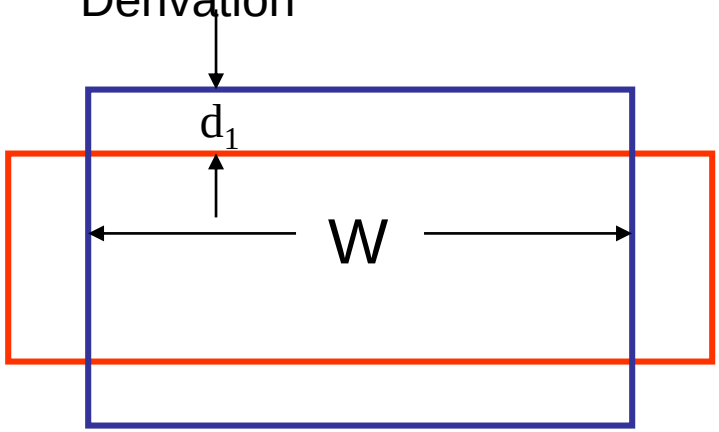
- Are there any structures that are more settling energy efficient than than of the basic amplifier?

➢ Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

- Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

Derivation



Layout of simple MOS Transistor

$$C_{DBn} = C_{BOTn} d_1 W_n + 2C_{SWn}\left(d_1 + W_n\right) = W_n\left(C_{BOTn} d_1 + 2C_{SWn}\right) + 2C_{SWn} d_1$$

$$C_{DBp} = C_{BOTp} d_1 W_p + 2C_{SWp}\left(d_1 + W_p\right) = W_p\left(C_{BOTp} d_1 + 2C_{SWn}\right) + 2C_{SWp} d_1$$

$$C_{TOT} = C_L + W_n\left(C_{BOTn} d_1 + 2C_{SWn}\right) + W_p\left(C_{BOTp} d_1 + 2C_{SWn}\right) + 2d_1\left(C_{SWp} + C_{SWn}\right)$$

$$C_{TOT} = C_L + \frac{P}{V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}^2}\left(\frac{C_{BOTn} d_1 + 2C_{SWn}}{L_{MIN} C_{OX}}\right) + \frac{L_{MIN}^2}{\mu_p V_{EB3}^2}\left(\frac{C_{BOTp} d_1 + 2C_{SWn}}{L_{MIN} C_{OX}}\right)\right] + 2d_1\left(C_{SWp} + C_{SWn}\right)$$

Define C_X by

$$C_X = \frac{\left(C_{SW} + C_{BOT}\, d_1\right)}{L_{MIN} C_{OX}}$$

$$\omega_T = 2\pi f_T = \frac{\mu V_{EB}}{L_{MIN}^2}$$

$$C_{TOT} = C_L + 2d_1\left(C_{SWp} + C_{SWn}\right) + \frac{P}{V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}^2} C_{Xn} + \frac{L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]$$

$$GB = \frac{g_{m1}}{2C_{TOT}} = \frac{I_T}{2C_{TOT} V_{EB1}} = \frac{P}{2V_{DD} C_{TOT} V_{EB1}}$$

Assumption: $W \gg d_1$

$$GB = \frac{1}{2V_{DD}} \frac{P}{V_{EB1}\left(C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)\right) + \frac{P}{V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

for TSMC 0.25u

C_{Xn} = .83

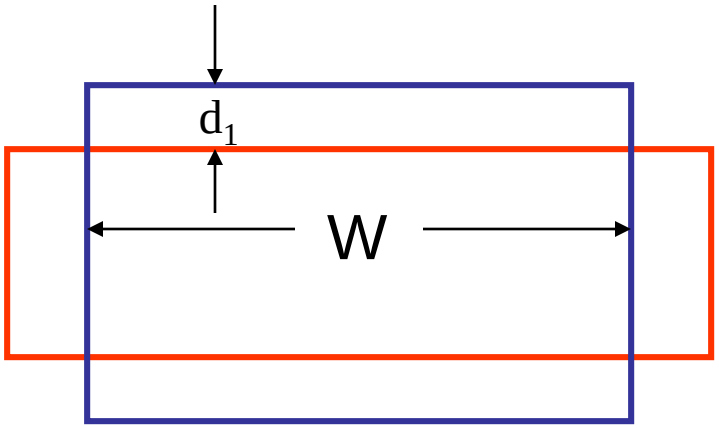
C_{Xp} = .90

where:

- C_{SW} is the sidewall capacitance density
- C_{BOT} is the bottom diffusion capacitance density
- L_{MIN} is the minimum gate length
- d_1 is the minimum spacing from poly to diffusion

Note: C_X is a dimensionless process parameter

Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?



Layout of simple MOS Transistor

Define C_X by

$$C_X = \frac{(C_{SW} + C_{BOT}\, d_1)}{L_{MIN} C_{OX}}$$

$$\omega_T = 2\pi f_T = \frac{\mu V_{EB}}{L_{MIN}^2}$$

Assumption: $W >> d_1$

where:

- C_{SW} is the sidewall capacitance density
- C_{BOT} is the bottom diffusion capacitance density
- L_{MIN} is the minimum gate length
- d_1 is the minimum spacing from poly to diffusion

for TSMC 0.25u
C_{Xn} = .83
C_{Xp} = .90

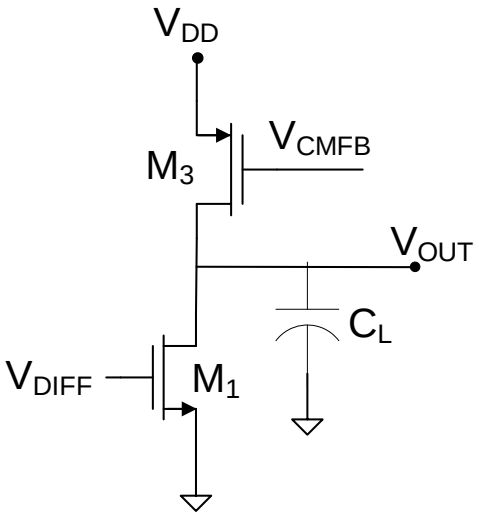
Note: C_X is a dimensionless process parameter

Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

for differential output 5T op amp ⇒ $GB = \frac{P}{2V_{DD}C_{TOT}V_{EB1}}$

Differential Half-Circuit for Basic Op Amp

$$DOF = \{V_{EB1}, V_{EB3}, P\}$$



By adding parasitic diffusion capacitances, it can be shown that

$$GB = \frac{1}{2V_{DD}} \frac{P}{V_{EB1}\left(C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)\right) + \frac{P}{V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

or in terms of the f_T parameters of the process as

$$GB = \frac{1}{2} \frac{P}{V_{DD}\left[V_{EB1}C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)\right] + P\left[\frac{C_{Xn}}{\omega_{Tn}} + \frac{C_{Xp}}{\omega_{Tp}} \frac{V_{EB1}}{V_{EB3}}\right]}$$

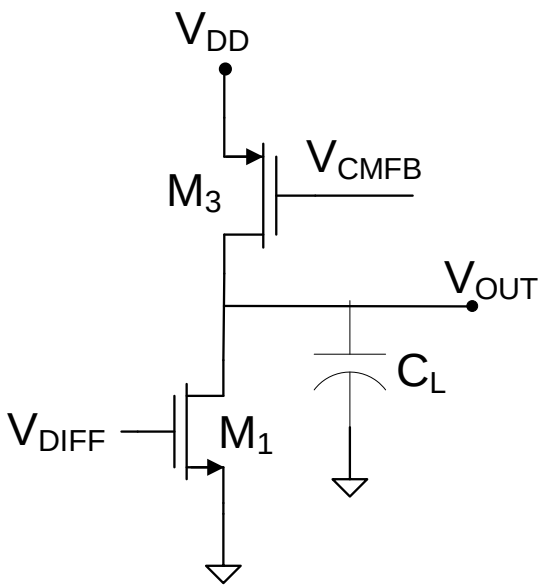
$$C_{TOT} = C_L + C_{PAR}$$

where ω_T is the f_T of the process in rad/sec

Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

Differential Half-Circuit for Basic Op Amp

$$DOF = \{V_{EB1}, V_{EB3}, P\}$$



$$GB = \frac{1}{2V_{DD}} \frac{P}{V_{EB1}\left(C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)\right) + \frac{P}{V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

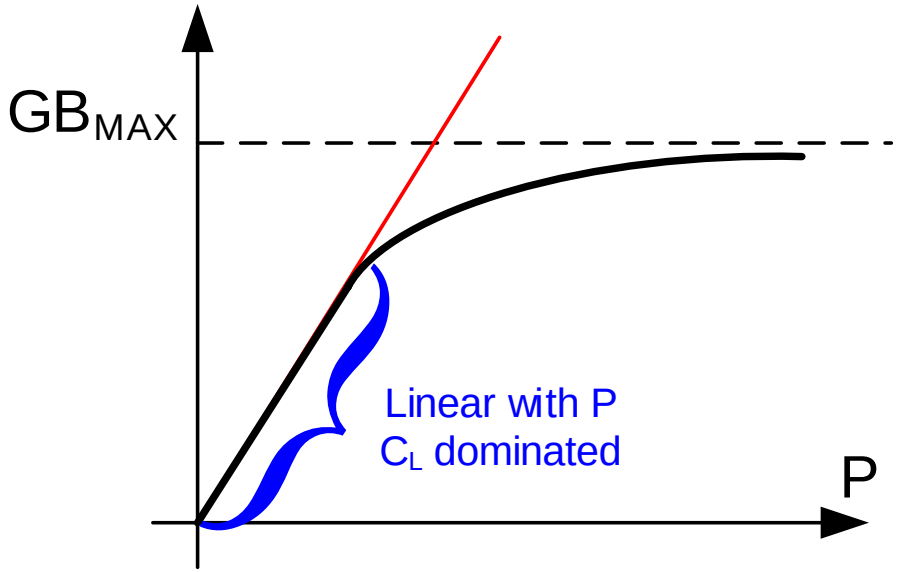
$$FOM = \frac{1}{4} \frac{1}{V_{EB1}\left(1 + 2d_1 \frac{C_{SWp} + C_{SWn}}{C_L}\right) + \frac{P}{C_L V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

$$C_{TOT} = C_L + C_{PAR}$$

$$FOM = \frac{GB \bullet V_{SUP} C_L}{2P}$$

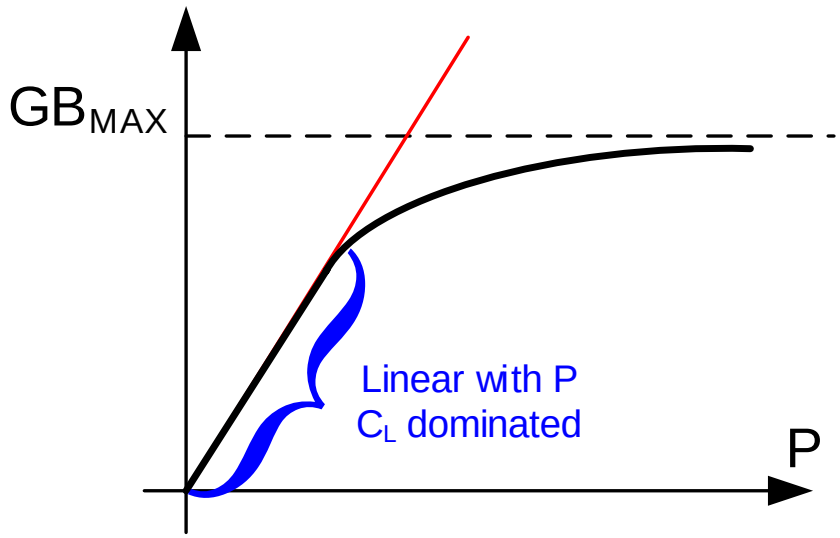
Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

$$GB = \frac{1}{2V_{DD}} \frac{P}{V_{EB1}\left(C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)\right) + \frac{P}{V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$



$$GB_{MAX} = \frac{1}{2} \frac{1}{\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?



No – reach a point of diminishing returns as power is increased

GB_{MAX} independent of C_L

What is a practical point of diminishing returns?

$$GB_{CRIT} = \frac{GB_{MAX}}{2} = \frac{1}{4\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

Settling Energy Efficiency of Popular Op Amps

Questions:

- Are there any structures that are more settling energy efficient than than of the basic amplifier?

- Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?

➢ Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

Recall:

$$\omega_T = \frac{\mu V_{EB}}{L_{MIN}^2}$$

Implication:

Speed increases with V_{EB}

Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

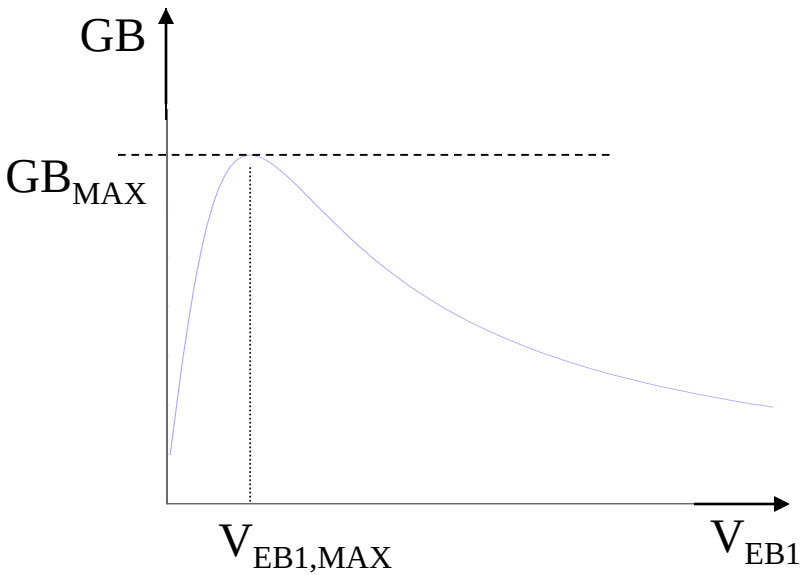
$$GB = \frac{1}{2V_{DD}} \frac{P}{V_{EB1}\left(C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)\right) + \frac{P}{V_{DD}}\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

$$DOF = \left\{V_{EB1}, V_{EB3}, \ P\right\}$$

To maximize GB, want to make V_{EB3} as large as possible without causing signal swing problems

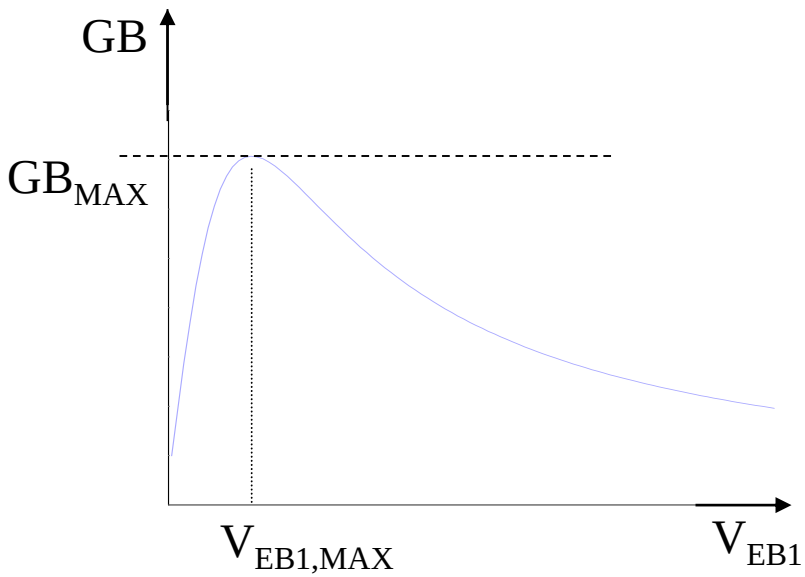
Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

No – but an optimal value of V_{EB1} can be obtained



$$V_{EB1,MAX} = \sqrt{\frac{1}{\dfrac{C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)}{\dfrac{P}{V_{DD}}\dfrac{L_{MIN}^2}{\mu_n}C_{Xn}} + \left[\dfrac{\mu_n C_{Xp}}{\mu_p C_{Xn} V_{EB3}^2}\right]}}$$

Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?



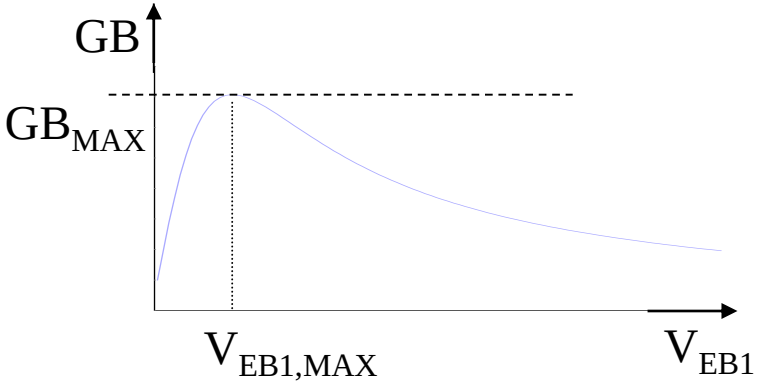
For large P, obtain

$$V_{EB1,MAX} = V_{EB3}\sqrt{\frac{\mu_p C_{Xn}}{\mu_n C_{Xp}}}$$

Substituting into GB_{MAX} expression, obtain

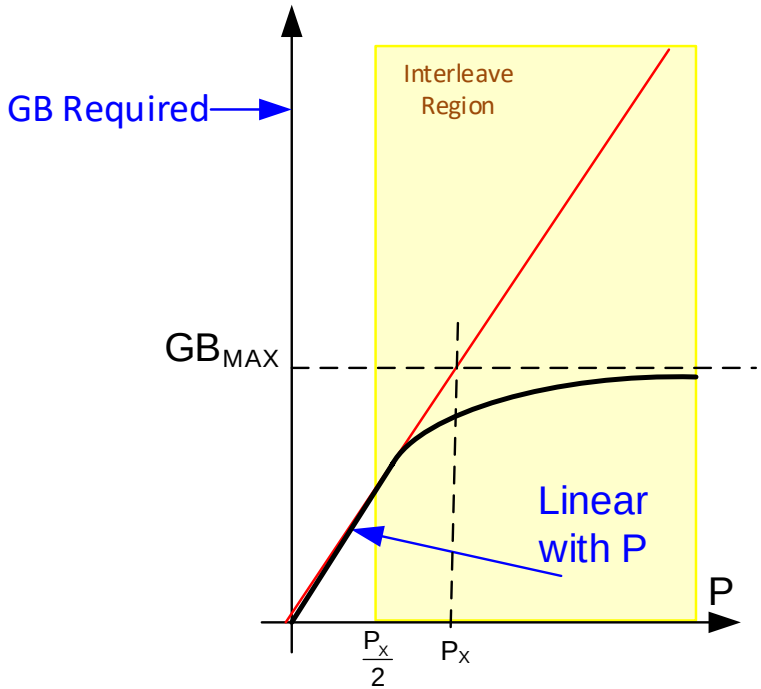
$$GB_{MAX} = \frac{\sqrt{\frac{\mu_n \mu_p}{C_{Xn} C_{Xp}}}\, V_{EB3}}{4L_{MIN}^2} = \frac{\omega_{Tp}}{4\sqrt{C_{Xn} C_{Xp}}}\sqrt{\frac{\mu_p}{\mu_n}}$$

Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?



$$GB_{MAX} = \frac{\omega_{Tp}}{4\sqrt{C_{Xn}C_{Xp}}}\sqrt{\frac{\mu_p}{\mu_n}}$$

If GB_{MAX} is not high enough, interleaving may provide a viable solution in a given technology node



Settling Energy Efficiency of Popular Single-Stage Op Amps

- ✓ Other single-stage op amps have settling performance properties similar to those considered here
- ✓ Increasing power improves settling time but a point of diminishing returns will limit the benefits
- ✓ Maintain large V_{EB3} to minimize effects of parasitics associated with p-channel transistor
- ✓ Set V_{EB1} at critical point to maximize GB for a given power dissipation

Energy Efficiency of Popular Single-Stage Op Amps

- Basic Single-Stage Diff Amp
- Current Mirror Op Amp
- Telescopic Cascode
- Folded Cascode
- Gain-Boosted Telescopic Cascode
- Gain-Boosted Folded Cascode
- -gm Compensated Single-Stage
- Telescopic Cascode Positive Feedback

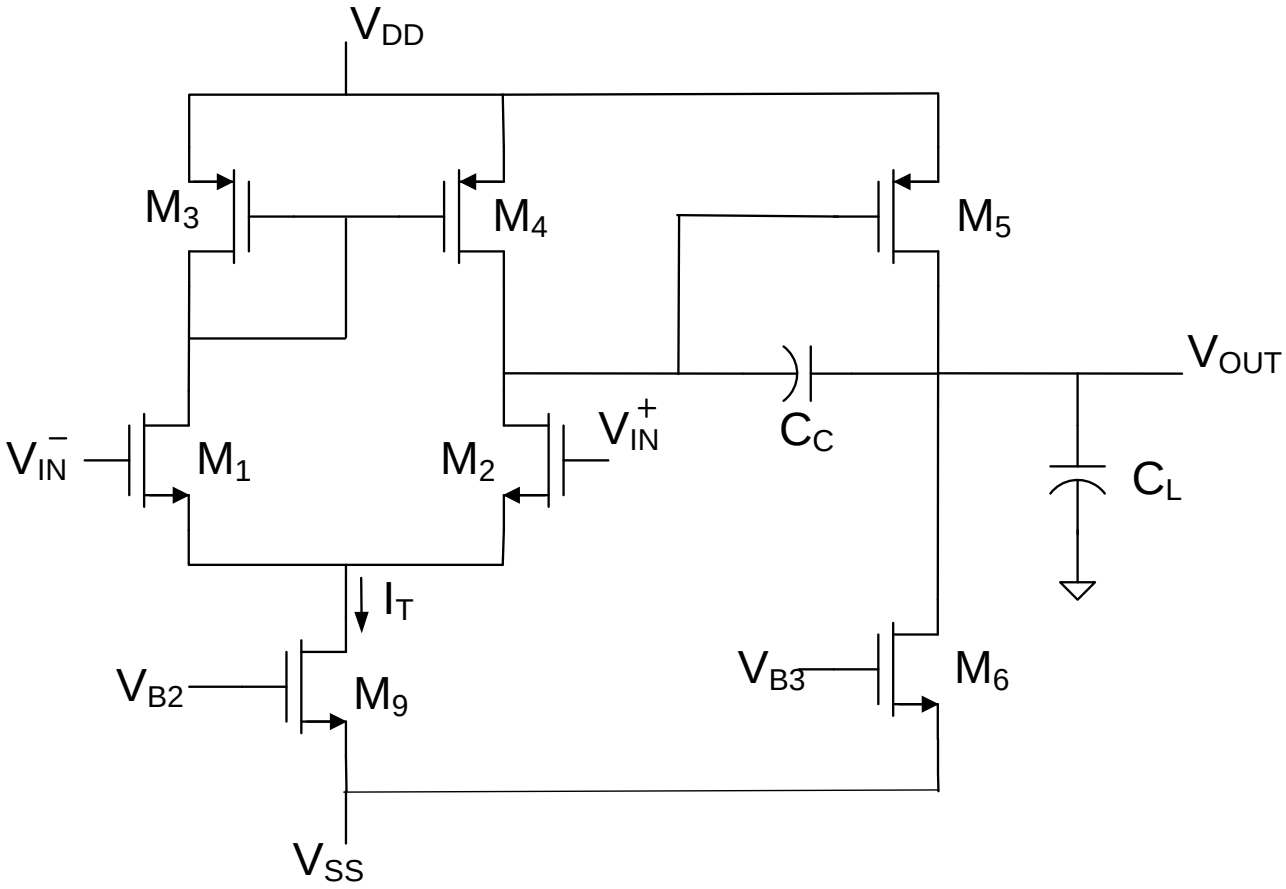
What about the 2-stage structures?

Energy Efficiency of Popular Two-Stage Op Amps

- Basic Two-Stage
- Cascode-Cascade
- Cascode-Cascode
- Telescopic Positive Feedback Cascode-Cascade
- -gm gain enhancement

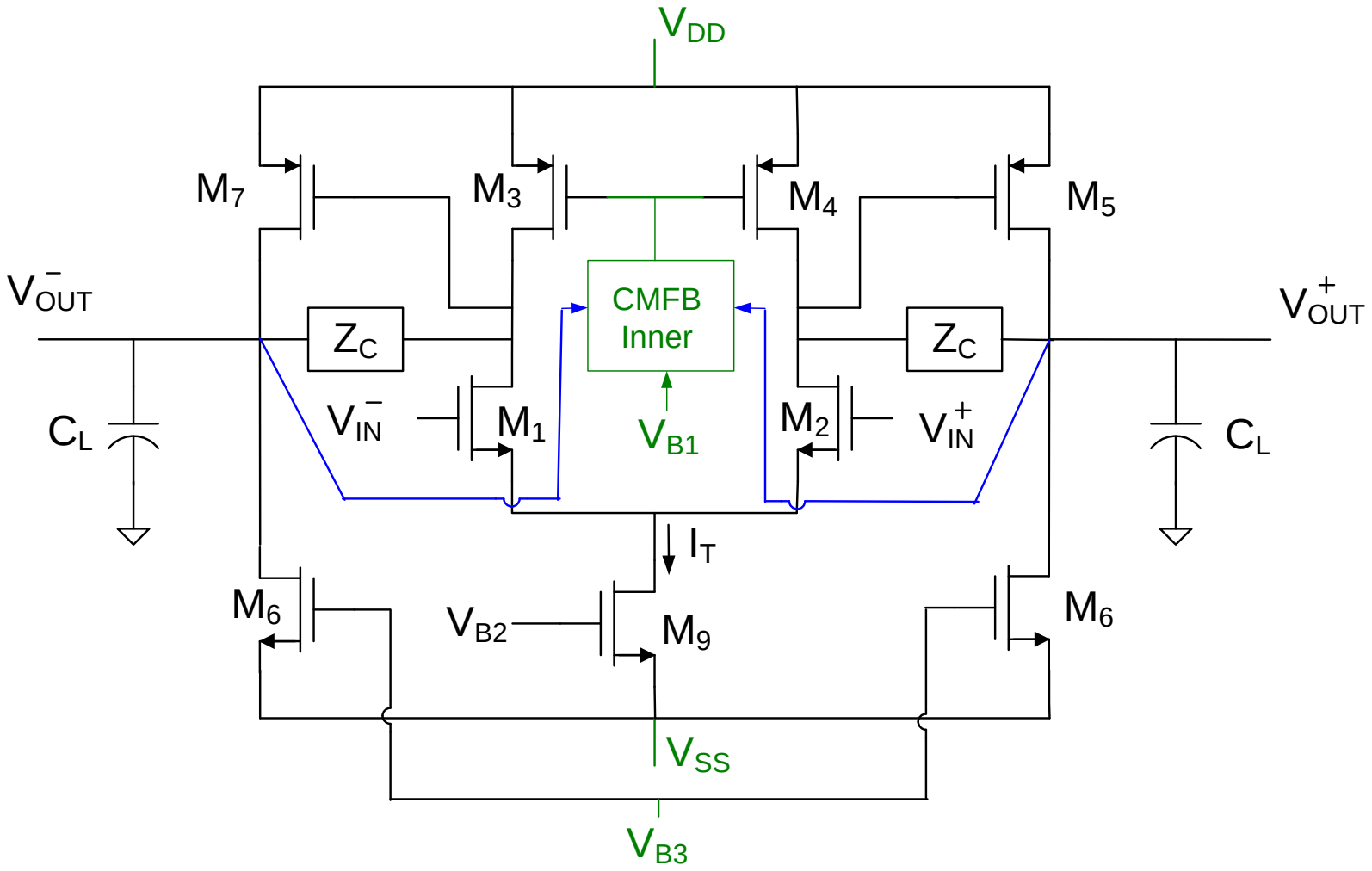
What about the 2-stage structures?

Two-Stage



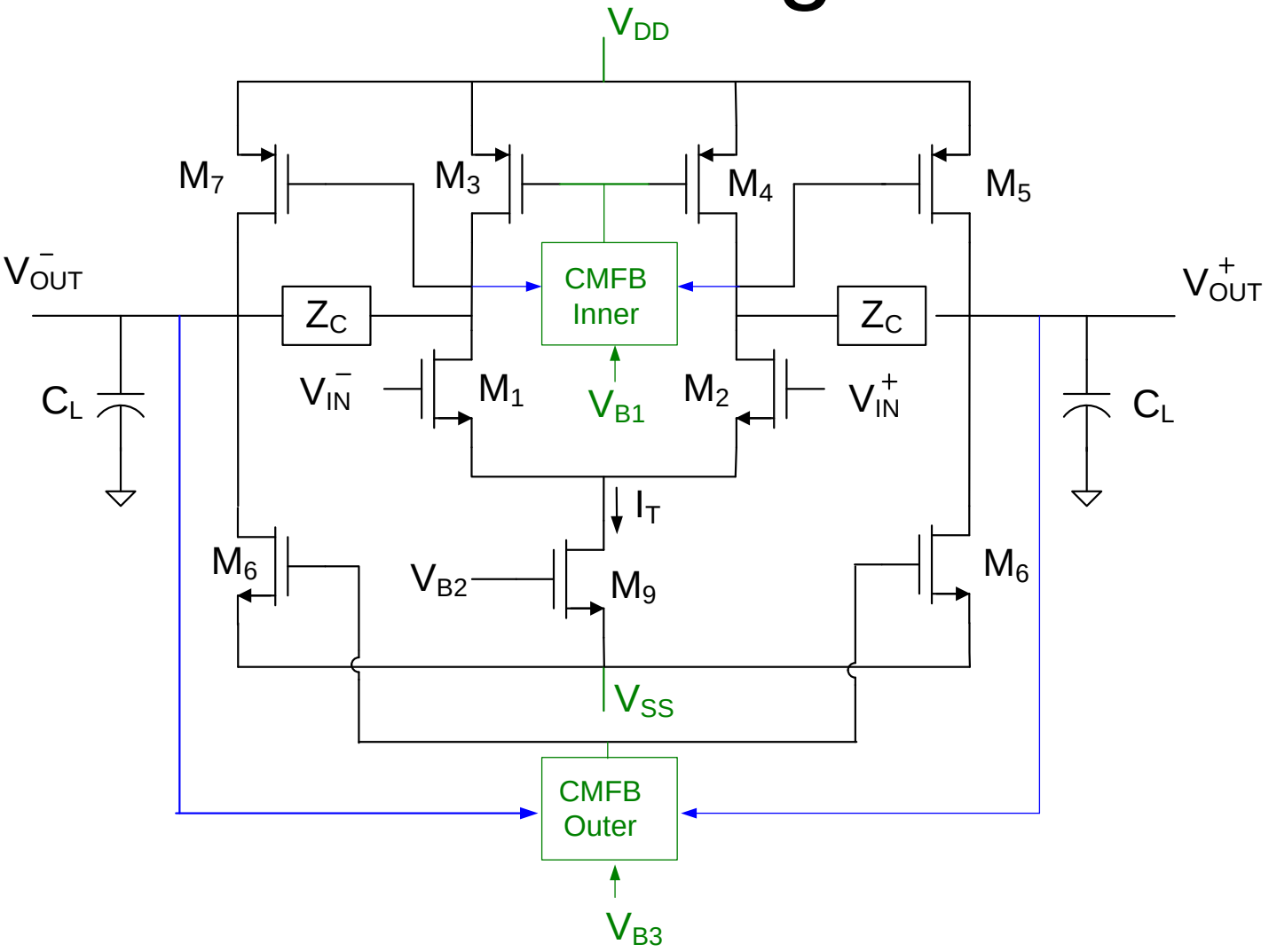
Single-Ended Output

Two-Stage



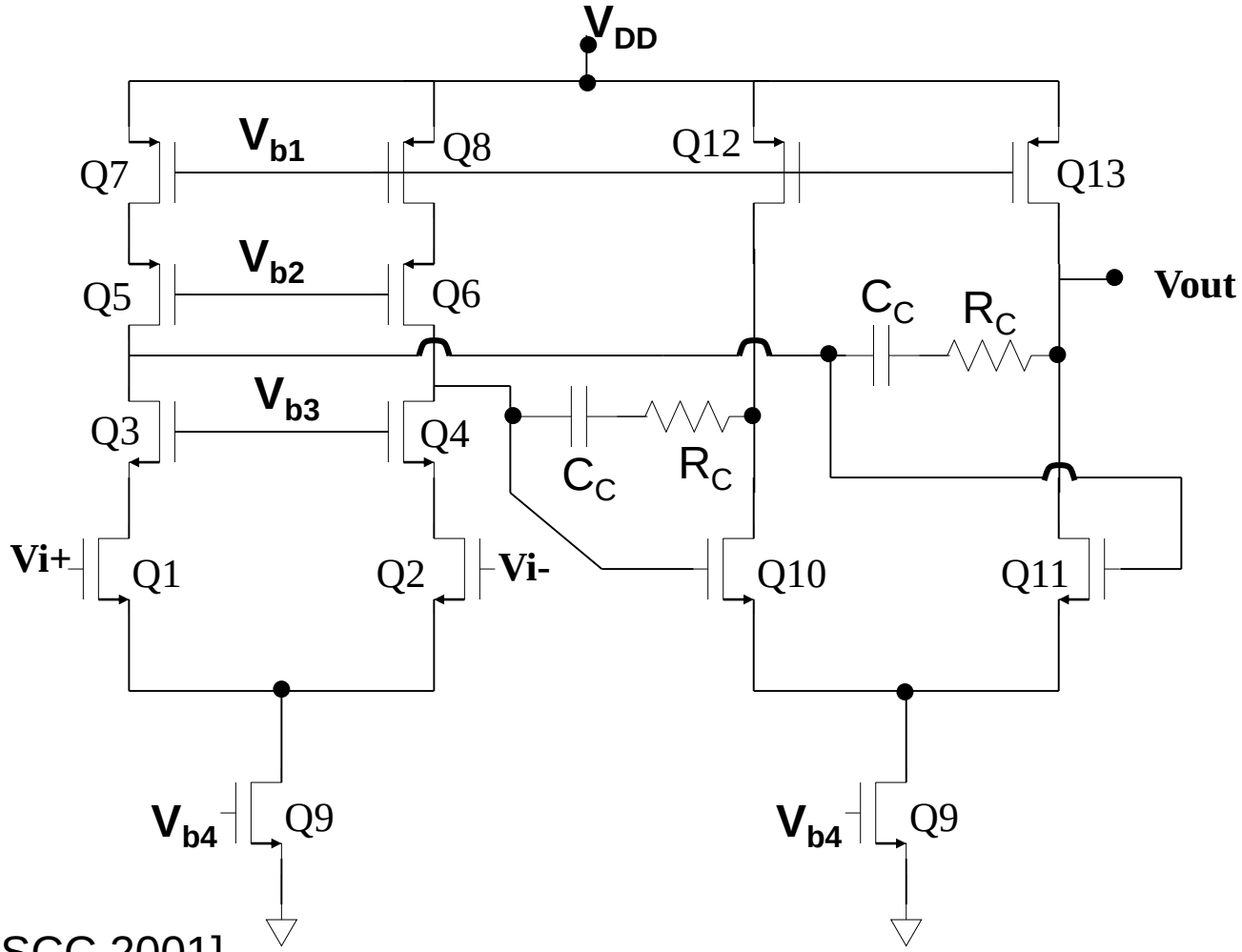
Fully Differential

Two-Stage



Fully Differential

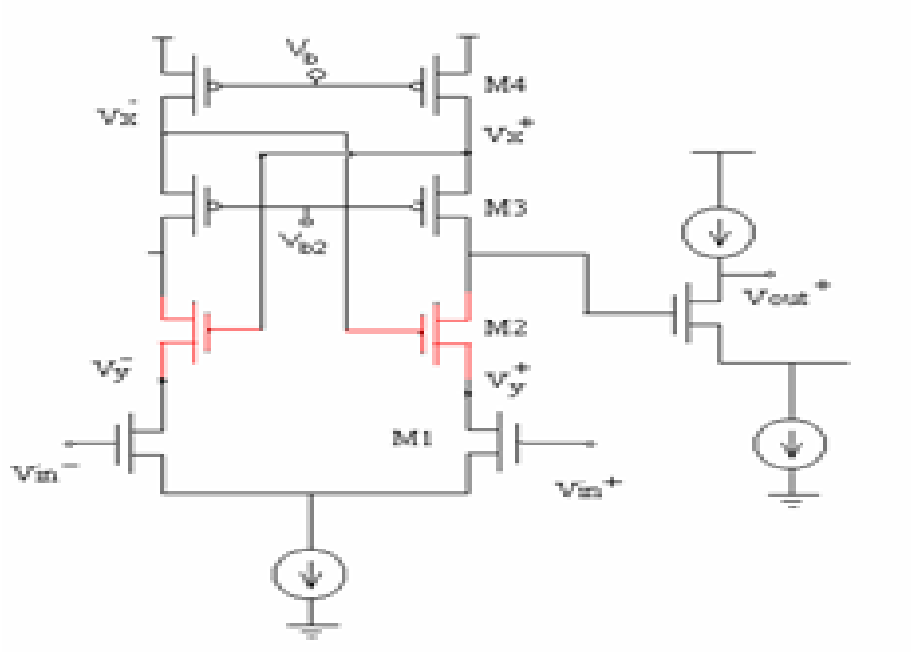
Two-Stage Cascode/Cascade



[Park – ISSCC 2001]

CMFB Not Shown

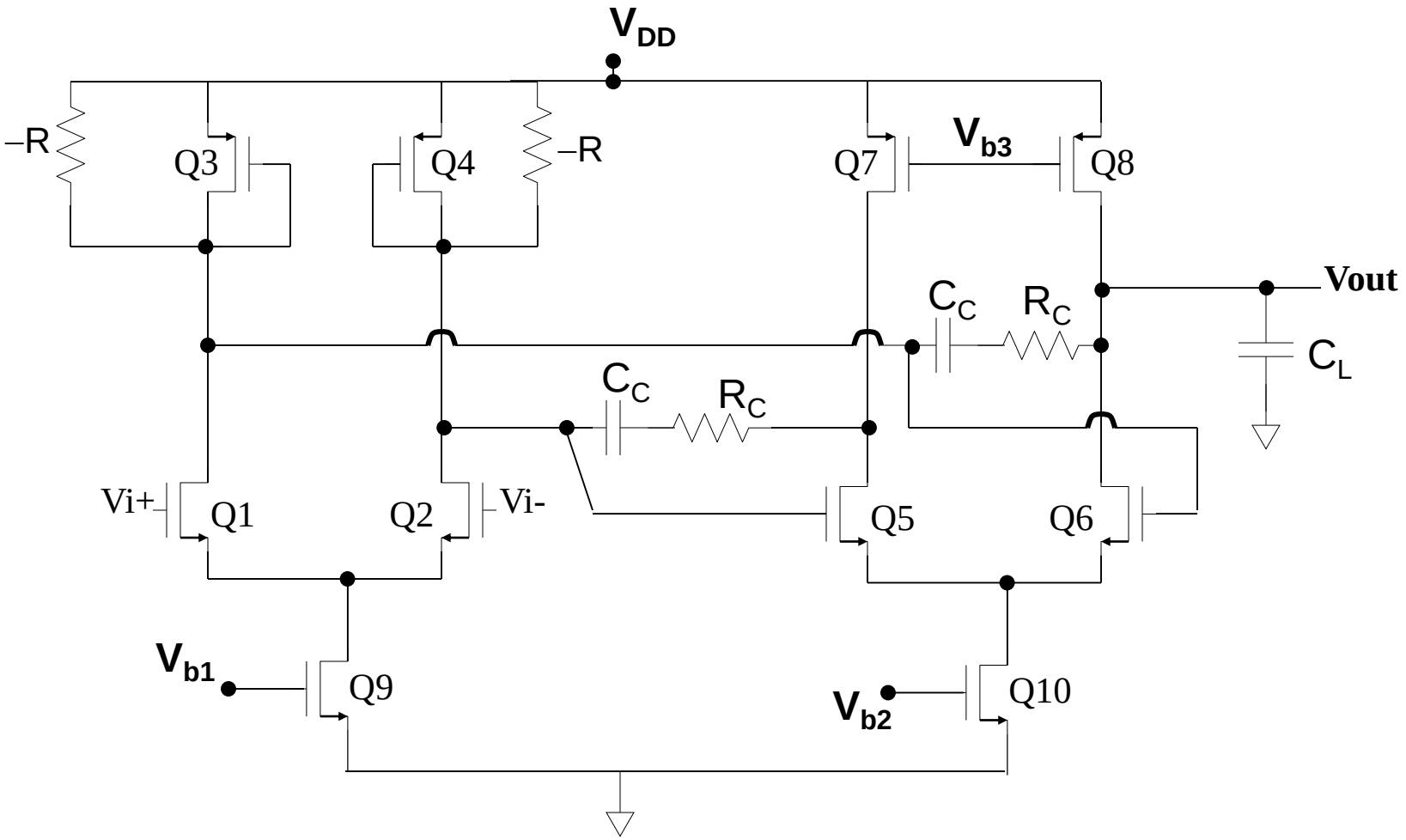
Telescopic Cascode Two-Stage Positive Feedback Op Amp



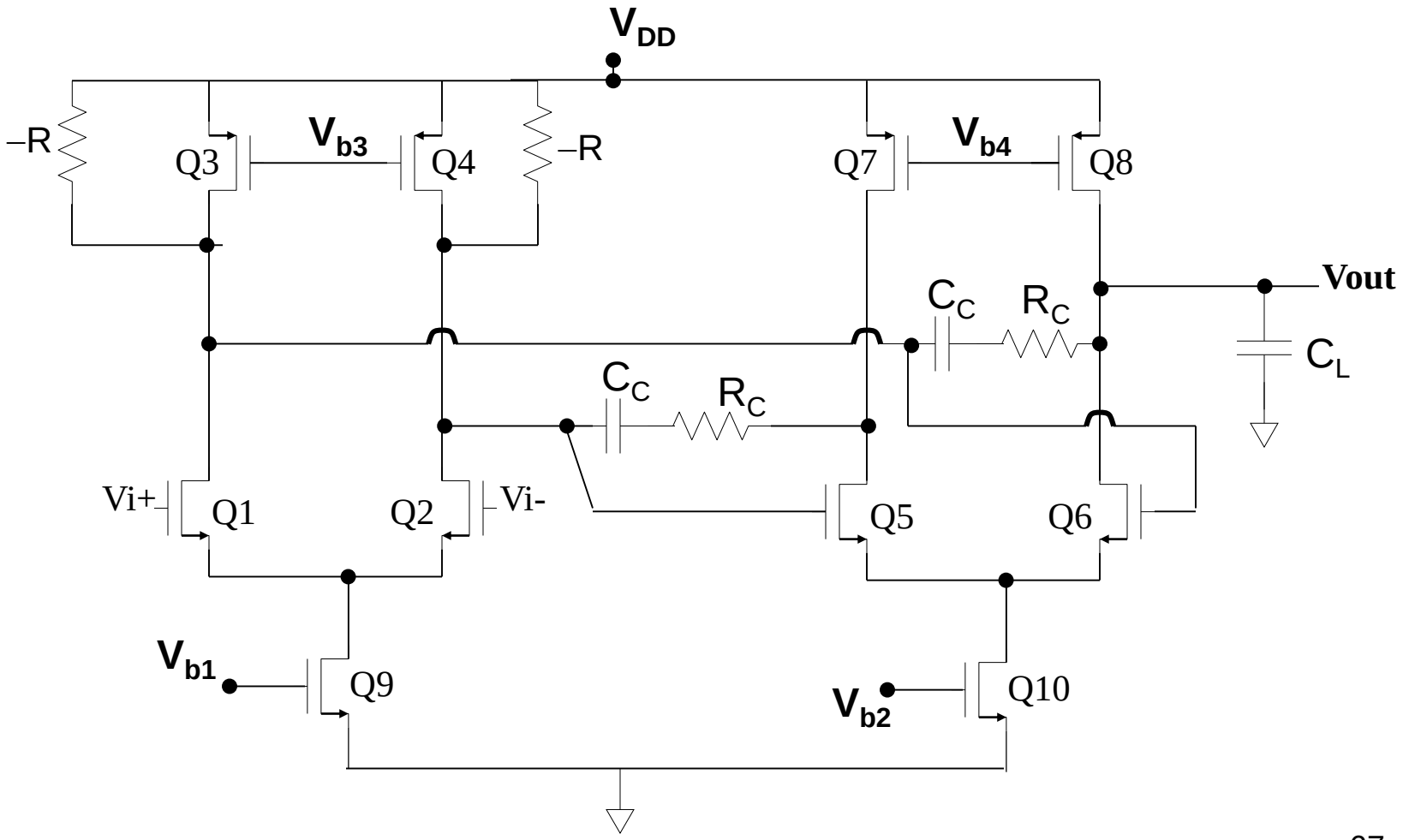
$$A_v \approx \left[\frac{-g_{m1}\cdot g_{m2}\cdot g_{m3}}{g_{o1}\left(g_{o2}\cdot g_{m3}-g_{o3}\cdot g_{m2}\right)}\right]\bullet\left[\frac{g_{m7}}{g_{07}+g_{o8}}\right]$$

CMFB Not Shown

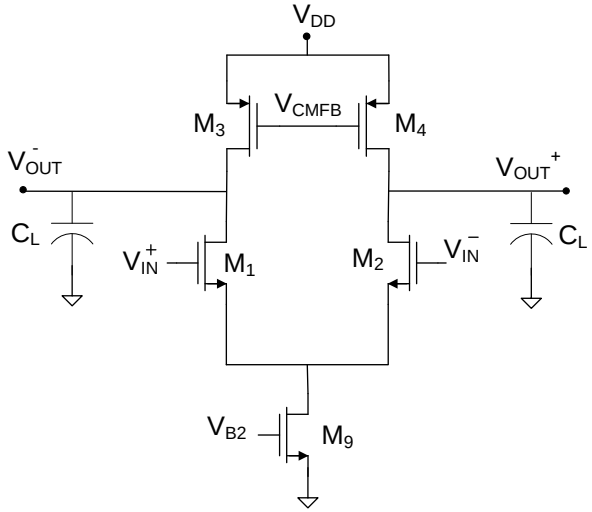
Two-Stage Negative R Compensation



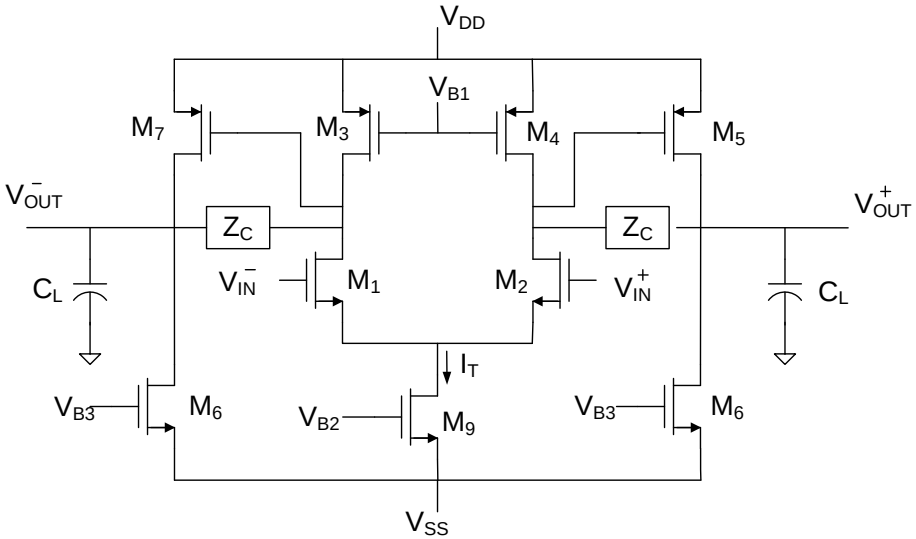
Enhanced-Gain Two-Stage Negative R Compensation



Improved Energy Efficiency Op Amps



OR ?



For some closed-loop gains the two-stage op amp is more power efficient than the single-stage Op Amp

See ISCAS 2005

Power Dependence of Feedback Amplifiers on OpAmp Architecture

Vipul Katyal, Yu Lin and Randall L. Geiger

Stay Safe and Stay Healthy !

End of Lecture 25